LED DRIVER WITH BUILD-IN POWER MOSFET SWITCH AND AVERAGE-MODE CONSTANT CURRENT CONTROL (functional analog HV9922 Supertex Inc.)

The IZ9922A is a pulse width modulated (PWM) LED driver control 1C. It allows efficient
operation of low current LED strings from voltage sources ranging up to 400VDC. The IZ9922A include an internal high-voltage switching MOSFET controlled with fixed off-time T_{OFF} of approximately 10us. The LED string is driven at constant current, providing constant light output and enhanced reliability. The output current is internally fixed at 50mA. The IZ9922A does not produce a peak-to-average error, and therefore greatly improves accuracy of the LED current. The IZ9922A designed for using low inductance value (typically 4.7mH for VLED=30V or 8 LEDs).

The average current control scheme of the IZ9922A provide good LED current regulation throughout the universal AC input voltage range of 85 to 264 VAC or DC input voltage of 20 to 400V.

FEATURES:

- Operating temperature range -40°C... +85 °C
- ON-resistance of the MOSFET switch 210 Ohm
- OFF-state breakdown voltage of the MOSFET switch not less 500 V
- Low inductance value (low cost)

APPLICATIONS:

- Decorative Lighting
- Low Power Light Fixtures
- LED Signs and Displays
- Architectural Lighting
- Incandescent Replacements
- Industrial Lighting

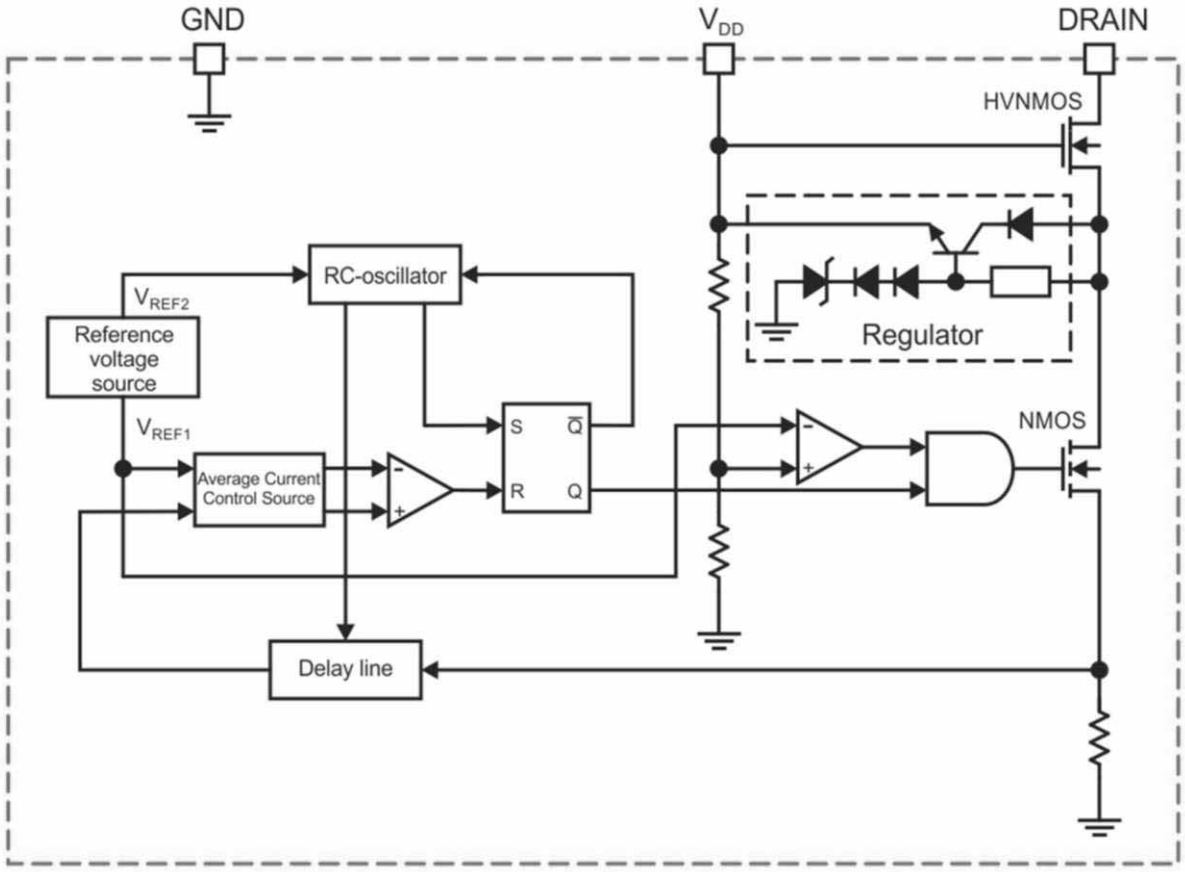


Figure 1 - Block diagram

Table 1 - Contact pad description

Contact pad number	Symbol	Description
01	TST	Test pad
02	PR3	Test pad
03	PR2	Test pad
04	TR	Test pad
05	PR1	Test pad
06	PR4	Test pad
07	Udd	Supply voltage pad
08	TU	Test pad
09	GND	Ground
10	PU1	Test pad
11	PU2	Test pad
12	PU3	Test pad
13	DRAIN	MOSFET switch drain pad
14	GND	Ground

Note:
1 Contact pad 01 - 06, 08, 10, 11, 12, 14 (test pads) are used for testing process on manufacturing fab only (have not to be bonded by customer).
2 Contact pad 09, 14 (Ground) are electrically connected

Table 2 - Recommended operation conditions

Symbol	Parameter	Min	Max	Unit
V_{DRAIN}	Input voltage	20	400	V

Table 3 - Absolute maximum rating

Symbol	Parameter	Min	Max	Unit
V_{DRAIN}	Input voltage	-0.3	420	V
V_{DD}	Low-voltage part supply voltage	-0.3	10	V

Table 4 - Electric parameters

Symbol	**Parameter**	**Test condition**	**Min**	**Max**	**Ambient temp., °C**	**Unit**
V_{DDR}	Regulator output voltage	V_{IN} = (20 * 400)V	5.5	9.0	25 ± 10	V
I_{DD}	Low-voltage (control) part of IC consumption current	V_{DD} = 9.5 V V_{DRAIN} = 40 V	-	350		
R_{ON}	ON-resistance of the switch (DRAIN)	$V_{DD} = U_{DDR}$ I_{DRAIN} = 20 mA	-	210		Ω
V_{UVLO}	Under voltage threshold (Low-voltage part of IC)	$V_{DD} = U_{UVLO}$ I_{DRAIN} = 50 mA	3.4	V_{DDR} - 0.3		V
I_{SAT}	MOSFET saturation current (DRAIN pin)	$V_{DD}= V_{DDR}$ V_{SAT} = 50 V	100	-		mA
V_{BR}	MOSFET switch breakdown voltage	$V_{DD} = V_{DDR}$ I_{DRAIN} = 1 mA	500	-		V

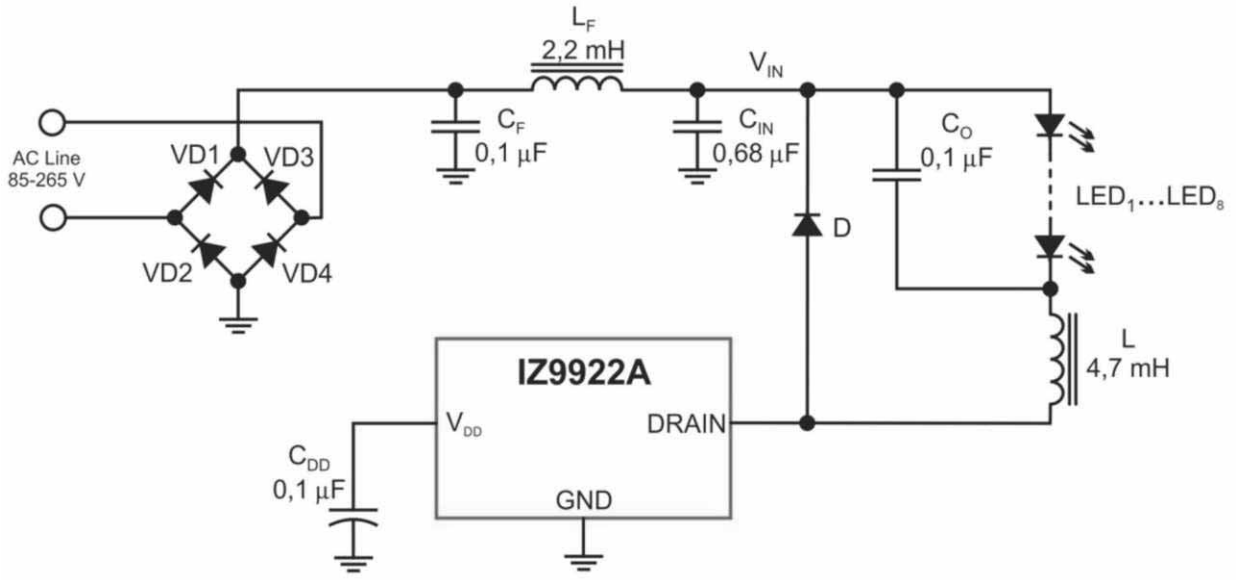
SYMBOL	Parameter	Test condition	Min	Max	Ambient temp., oC	Unit
I_{AVE}	Average current	$V_{DD} = V_{DDR}$	47.0	54.0	25 ± 10 -40 85	mA
T_{OFF}	OFF time (DRAIN)	$V_{DD} = V_{DDR}$	8.0	13.0	25 ± 10	ns
T_{ON}	Minimum ON-time of the switch (DRAIN)		-	650		
T_{BLANK}	Leading Edge Blanking Delay		200	400		ns

Functional Description

The IZ9922A is PWM average current controller for controlling a buck converter topology in continuous conduction mode (CCM). The output current is internally preset at 50 mA.

When the input voltage of 20 to 400 V appears at the DRAIN pin, the internal high-voltage linear regulator seeks to maintain a voltage of 7 VDC at the VDD pin. Until this voltage exceeds the internally programmed under-voltage threshold, the output DRAIN is non-conductive. When the threshold is exceeded, the DRAIN turns on. The input current begins to flow into the DRAIN pin. Hysteresis is provided in the under-voltage comparator to prevent oscillation. When the input current exceeds the internal preset level (from average current control source), a current sense comparator resets an RS flip-flop, and the DRAIN turns off. At the same time, a one-shot circuit is activated that determines the duration of the off-state (10 μS typ.). As soon as this time is over, the flip-flop sets again. The new switching cycle begins. A "blanking" delay of 300 nS is provided that prevents false triggering of the current sense comparator due to the leading edge spike caused by circuit parasitics.

Typical Application Circuit



Selecting L and D

The current through the switching MOSFET source is averaged and used to give constant-current feedback. It is a good practice to design the inductor such that the switching ripple current in it is + 50% of its average value (from 25 mA to 75 mA). Hence, the recommended inductance can be calculated as:

$$L = \frac{T_{OFF\_MIAX} * V_O}{I_{AVE}} \quad (1)$$

Vo is the forward voltage of the LED string. Toff is the off time of the IZ9922A.

The duty-cycle range of the current control feedback is limited to D < 0.75. A reduction in the LED current may occur when the LED string voltage V_O is greater than 75% of the input voltage V_{IN}.

Another important aspect of designing an LED driver with the IZ9922A is related to certain parasitic elements of the circuit, including distributed coil capacitance of L, junction capacitance and reverse recovery of the rectifier diode D, capacitance of the printed circuit board traces Cpcb and output capacitance Cdrain of the controller itself. These parasitic elements affect the efficiency of the switching converter and could potentially cause false triggering of the current sense comparator if not properly managed. Minimizing these parasitics is essential for efficient and reliable operation of the IZ9922A. Coil capacitance of inductors is typically provided in the manufacturer's data books either directly or in terms of the self-resonant frequency (SRF).

$$SRF = \frac{1}{(2\pi\sqrt{LC_L})} \quad (2)$$

where L is the inductance value, and C_L is the coil capacitance.

Charging and discharging this capacitance every switching cycle causes high-current spikes in the LED string. Therefore, connecting a small capacitor Co (~10 nF) is recommended to bypass these spikes. Using an ultra-fast rectifier diode for D is recommended to achieve high efficiency and reduce the risk of false triggering of the current sense comparator. Using diodes with shorter reverse recovery time t_{RR} and lower junction capacitance C_j achieves better performance. The reverse voltage rating V_R of the diode must be greater than the maximum input voltage of the LED lamp. The total parasitic capacitance present at the DRAIN pin of the IZ9922A can be calculated as:

$$C_P = C_{DRAIN} + C_{PCB} + C_L + C_J \quad (3)$$

where and CDRAIN is the DRAIN capacitance (CDRAIN < 5 pF), and CPSB is the printed-circuit board capacitance.

When the switching MOSFET turns on, the capacitance C_P is discharged into the DRAIN pin of the IC. The discharge current is limited to about 150 mA typically. However, it may become lower at increased junction temperature. The duration of the leading edge current spike can be estimated as:

$$T_{SPIKE} = t_{RR} + \frac{V_{IN} * C_P}{I_{SAT}} \quad (4)$$

In order to avoid false triggering of the current sense comparator, CP must be minimized in accordance with the following expression:

$$C_P < \frac{I_{SAT} * (T_{BLANK\_MIN} - t_{RR})}{V_{IN\_MAX}} \quad (5)$$

where T_{BLANK_MIN} is the instantaneous input voltage.

Estimating Power Loss

Discharging the parasitic capacitance CP into the DRAIN pin of the IZ9922A is responsible for the bulk of the switching power loss. It can be estimated using the following equation:

$$P_{SWITCH} = \left(\frac{V_{IN}^2 * C_P}{2} + V_{IN} * I_{SAT} * t_{RR} \right) * F_S \quad (6)$$

where F_S is the switching frequency, I_{SAT} is the saturated DRAIN current of the IZ9922A. The switching loss is the greatest at the maximum input voltage. The switching frequency is given by the following:

$$F_S \approx \frac{V_{IN} - V_O}{V_{IN} * T_{OFF}} \quad (7)$$

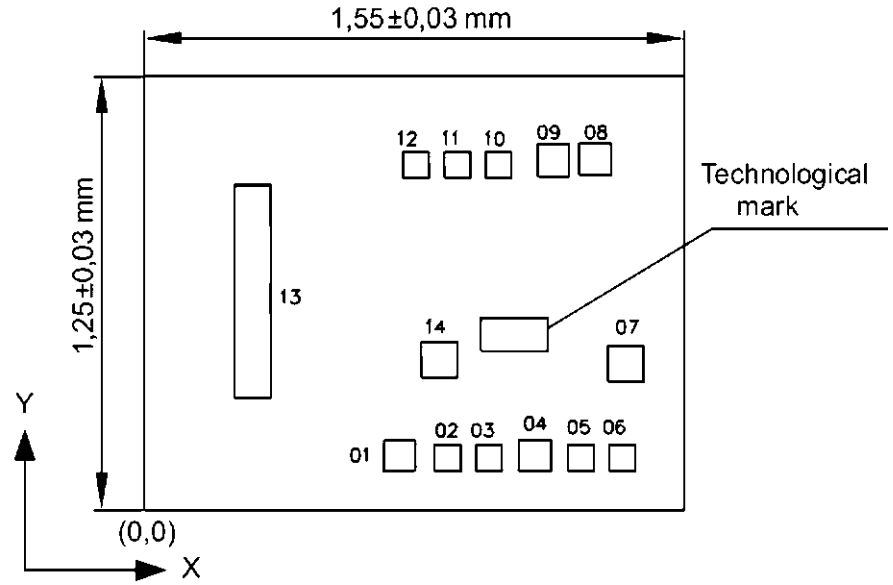
The switching power loss associated with turn-off transitions of the DRAIN pin can be disregarded. Due to the large amount of parasitic capacitance connected to this switching node, the turn-off transition occurs essentially at zero-voltage. Conduction power loss in the IZ9922A can be calculated as:

$$P_{COND} \approx I_O^2 * R_{ON} * \frac{V_O}{V_{IN}} + I_{DD} * (V_{IN} - V_O) \quad (8)$$

where R_{ON} is the ON resistance, IDD is the internal linear regulator current.

$$P_{TOTAL} = P_{SWITCH} + P_{COND} \quad (9)$$

Contact pad layout diagram



Die thickness 0.46±0.02 mm.
Technological mark coordinates, um: x=918, y=427.

Table 5 - Technological mark

Type of IC	Technological mark
IZ9922A	20 9922-2

Table 6 - Contact pad coordinates and sizes

Contact pad number	Coordinates (left bottom corner), um		Contact pad dimension, um
	X	Y	
01	665	110	85 x 85
02	804	110	70 x 70
03	928	110	70 x 70
04	1057	110	85 x 85
05	1201	110	70 x 70
06	1325	110	70 x 70
07	1306	345	95 x 95
08	1242	950	85 x 85
09	1096	950	85 x 85
10	966	965	70 x 70
11	860	965	70 x 70
12	754	965	70 x 70
13	246	273	95 x 570
14	774	356	95 x 95
Note - Contact pad coordinates and dimensions are indicated under "Passivation" layer			