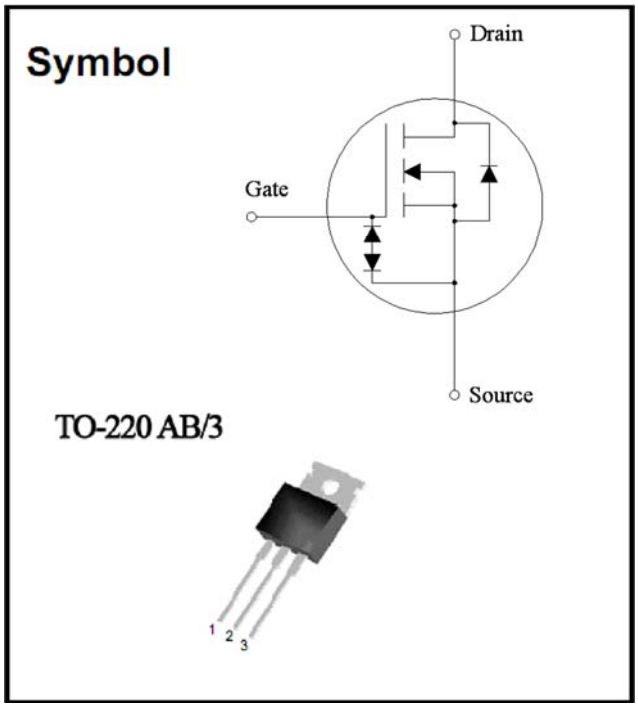
N-Channel 800 V power MOSFET



Features

- Zener- protected MOSFET
- 100% avalanche tested
- Gate charge minimized
- Typical $R_{DS(on)}$ = 1,9 Ω
- Maximum Junction Temperature Range (150 °C)

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DS}	Drain to Source Voltage	800	V
V_{GS}	Gate to Source Voltage	±30	V
I_D	Continuous Drain Current(@T_C = 25 °C)	4,7	A
	Continuous Drain Current(@T_C = 100 °C)	2,7	A
I_{DM} [1)]	Drain Current Pulsed	17,2	A
P_{TOT}	Total Power Dissipation(@T_C = 25 °C)	110	W
	Derating Factor above 25 °C	0,88	W/°C
E_{AS} [2)]	Single Pulsed Avalanche Energy	190	mJ
T_{STG}, T_J	Operating and Storage Temperature Range	-55 ~ +150	°C

1) Pulse width limited by safe operation area

2) V_{DD} = 50 V, I_D = 4,7 A , Starting T_J = 25 °C

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	-	1,14	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	-	62,5	°C/W

Gate-Source Zener Diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{GSO}	Gate-source breakdown voltage	I_{GS} = ± 1 mA (Open Drain)	30	-	-	V

Protection features of gate-to-sorce zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device`s ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device`s integrity. These integrated Zener diodes thus avoid the usage of external components.

Electrical Characteristics (T_C = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA	800	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 800 V, V_{GS} = 0 V	-	-	10	µA
		V_{DS} = 800 V, V_{GS} = 0 V T_C = 125 °C	-	-	100	µA
I_{GSS}	Gate-Source Leakage, Forward	V_{GS} = ±20 V	-	-	±10	µA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	3,75	4,5	V
$R_{DS(ON)}$	Static Drain-Source On-state Resis-tance	V_{GS} = 10 V, I_D = 2,15 A	-	1,9	2,4	Ω

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
g_{fs} [1]	Forward Transconductance	V_{DS} = 15 V, I_D = 2,15 A	-	4,5	-	S
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	-	1250	1400	pF
C_{oss}	Output Capacitance		-	95	140	
C_{rss}	Reverse Transfer Capacitance		-	15	30	
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 400 V, I_D = 2 A, R_G = 4,7 Ω, V_{GS} = 10 V	-	18	-	ns
t_r	Rise Time		-	25	-	
$t_{d(off)}$	Turn-off Delay Time		-	45	-	
t_f	Fall Time		-	30	-	
Q_g	Total Gate Charge	V_{DD} = 640 V, V_{GS} = 10 V, I_D = 4,7 A	-	32,5	45	nC
Q_{gs}	Gate-Source Charge		-	5	-	
Q_{gd}	Gate-Drain Charge(Miller Charge)		-	18	-	

[1] Pulsed: Pulse duration = 300 µs, duty cycle 1,5%

Source-Drain Diode Characteristics and Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{SD}	Source-Drain Diode Forward Current		-	-	4,7	A
I_{SDM} [1]	Pulsed Source-Drain Diode Forward Current		-	-	17,2	
V_{SD} [2]	Diode Forward Voltage	I_S = 4,7 A, V_{GS} = 0 V	-	-	1,6	V

[1] Pulse width limited by safe operation area

[2] Pulsed: Pulse duration = 300 µs, duty cycle 1,5%

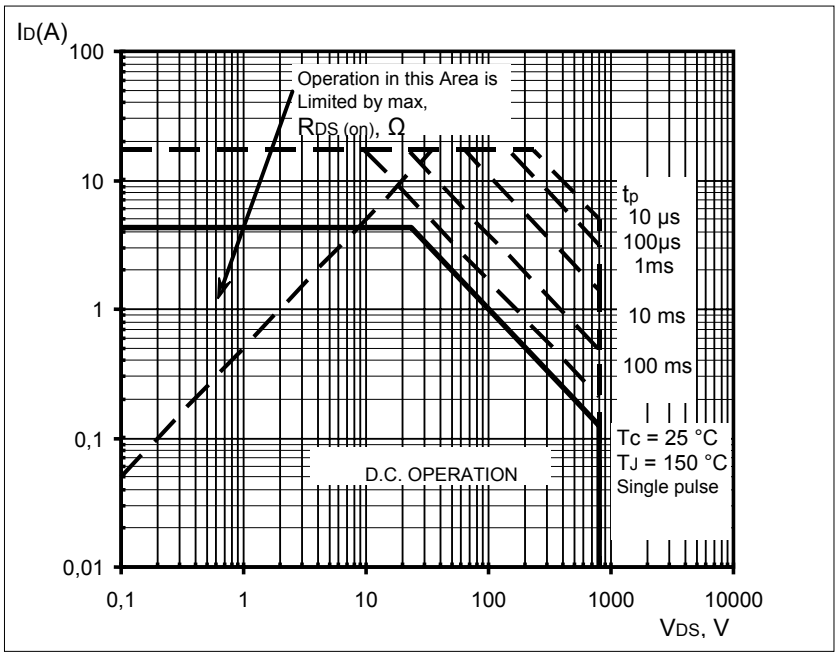


Figure 1 - Safe Operation Area

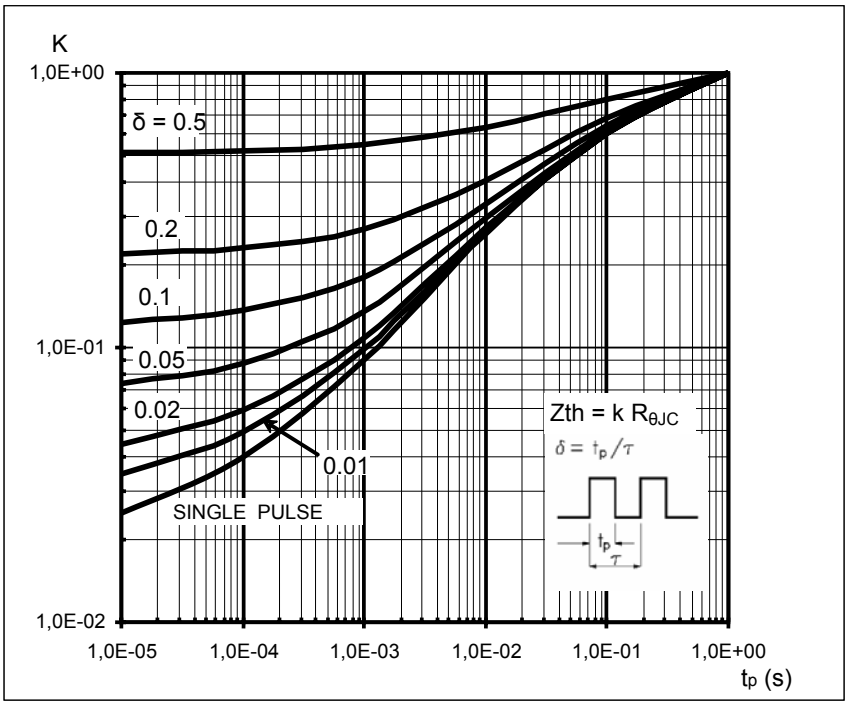


Figure 2 - Thermal Impedance

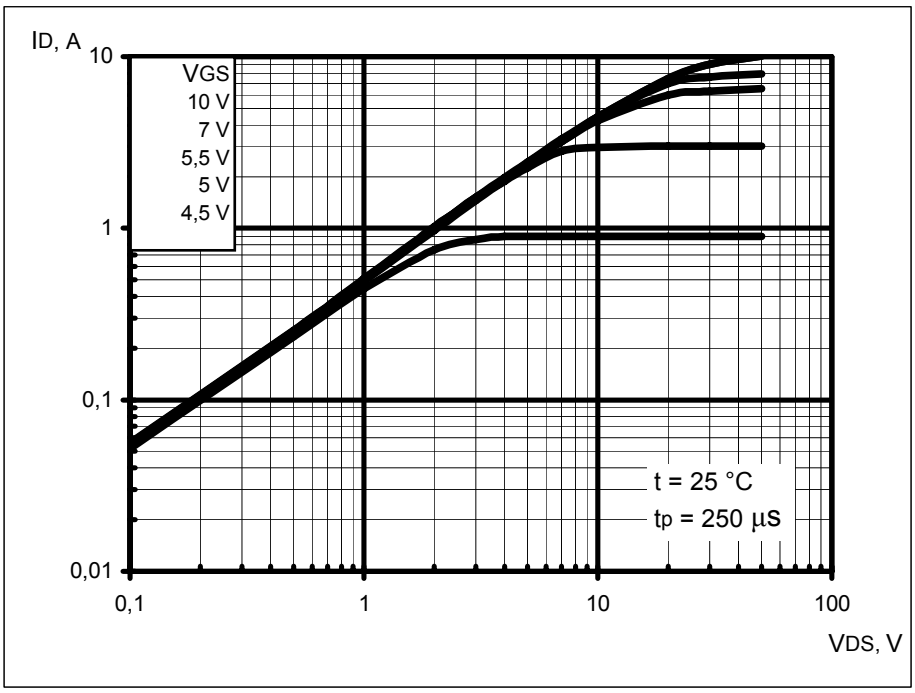


Figure 3 – Output characteristics

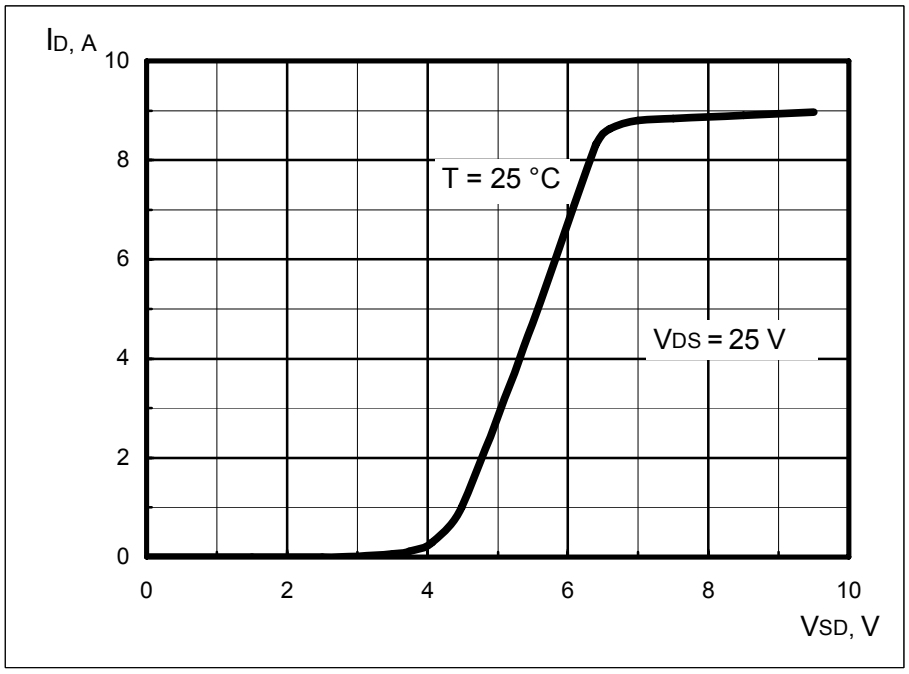


Figure 4 - Transfer Characteristics

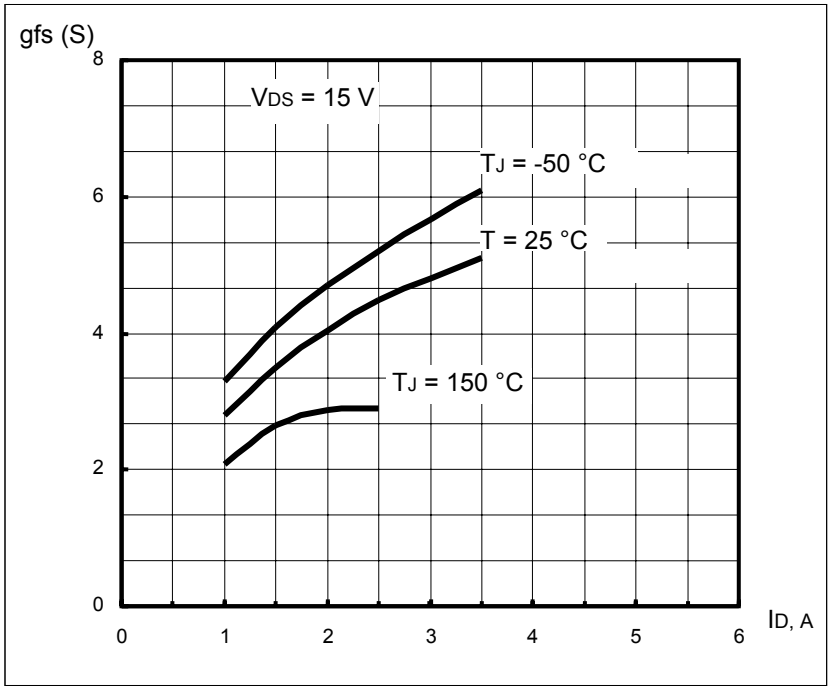


Figure 5 - Transconductance

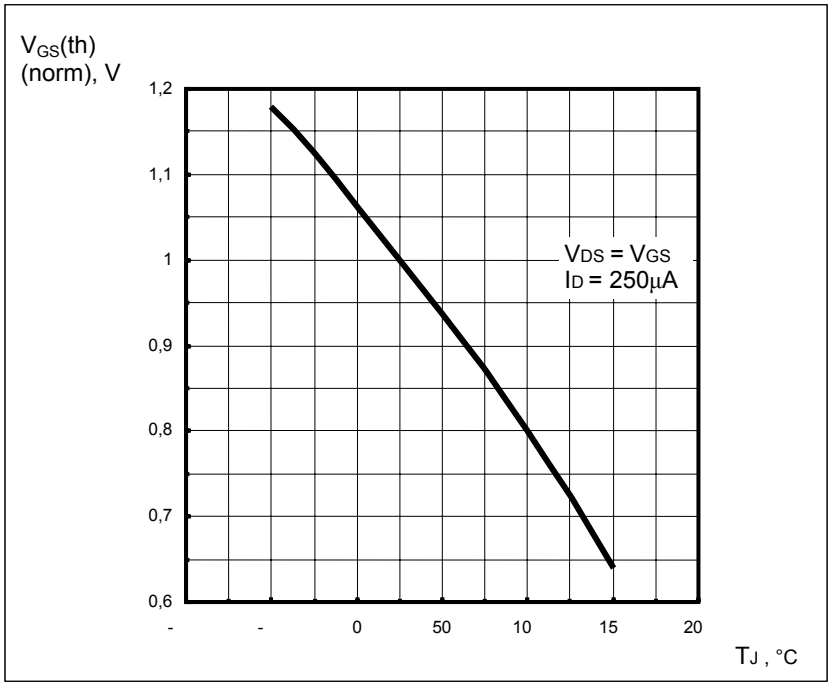


Figure 6 - Normalized Gate Threshold Voltage vs Temperature

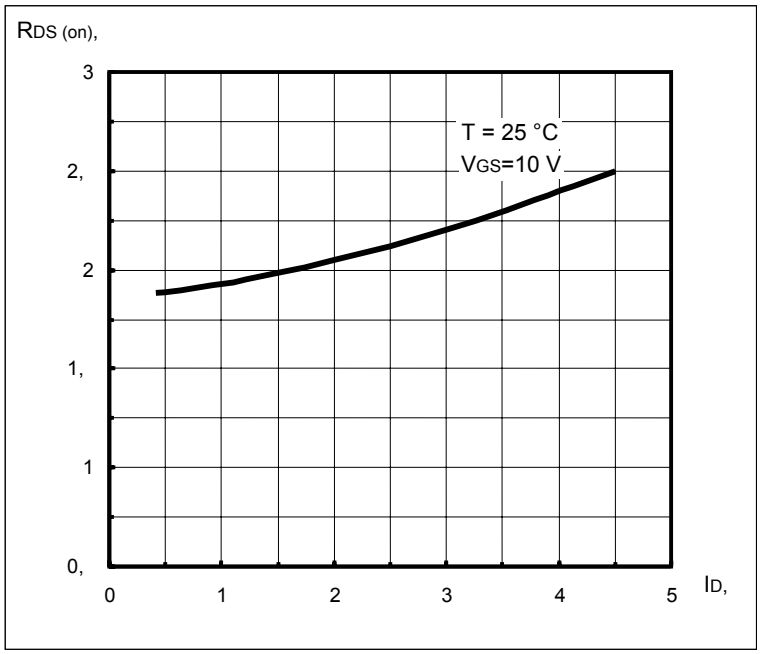


Figure 7 - Static Drain-source On Resistance

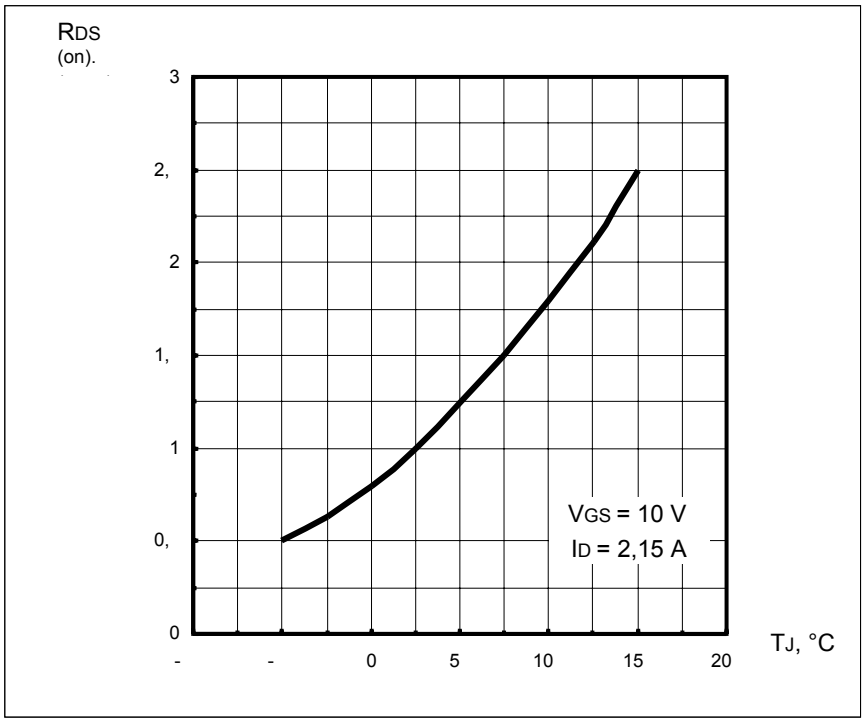


Figure 8 - Normalized On Resistance vs Temperature

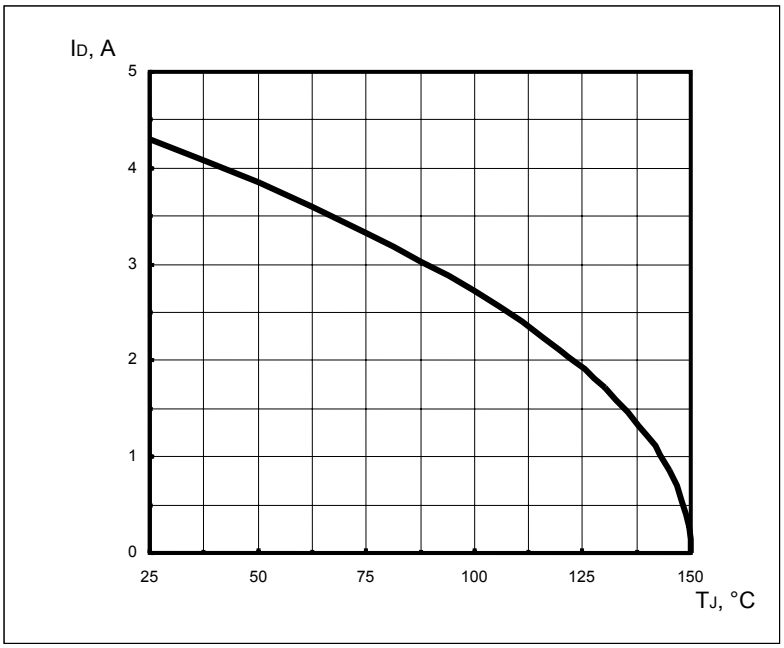


Figure 9 – Maximum Drain Current vs Case Temperature

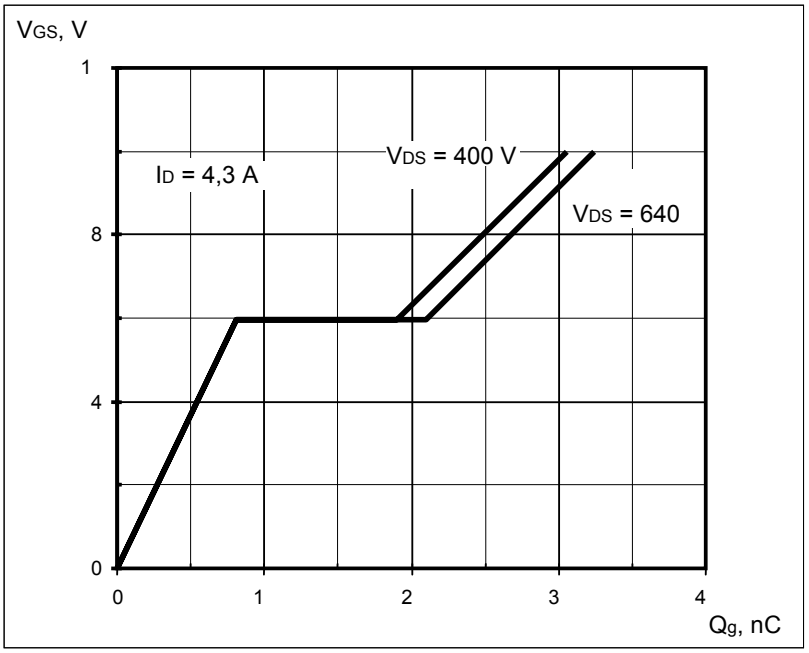


Figure 10 - Gate Charge vs Gate-source Voltage

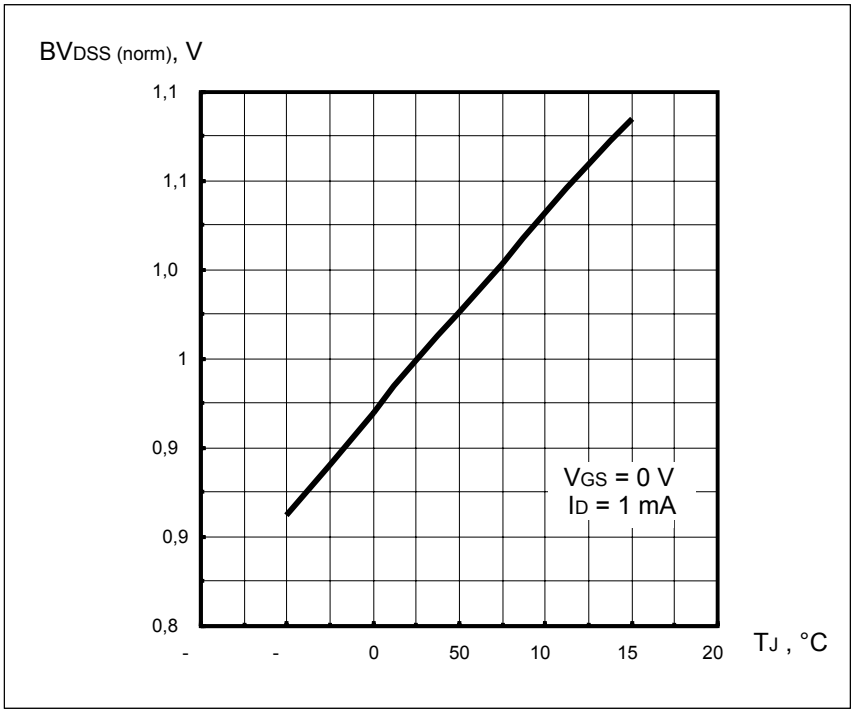


Figure 11 - Normalized BVDSS vs Temperature

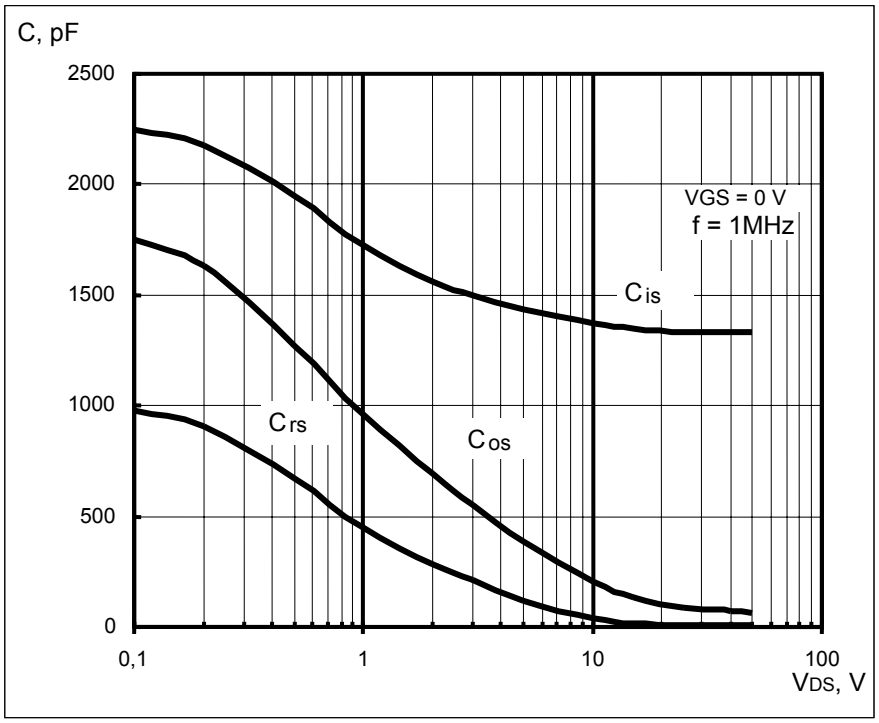


Figure 12 - Capacitance Varications

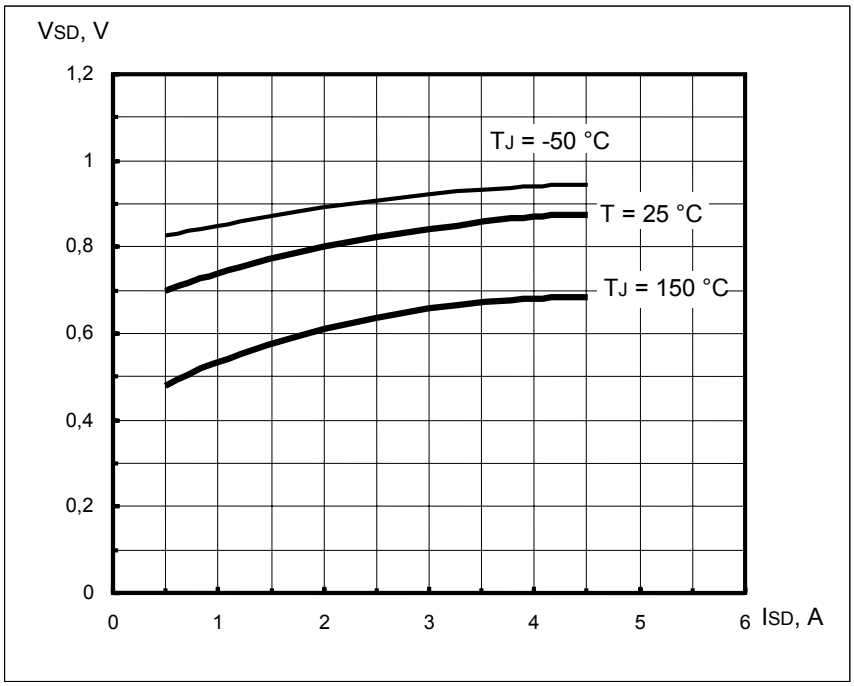


Figure 13 - Source-drain Diode Forward Characteristics

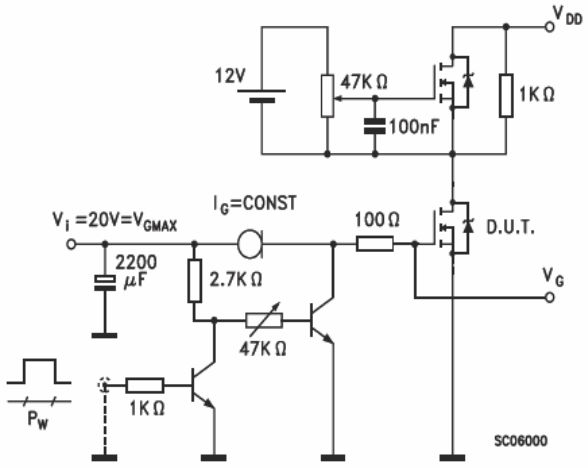


Figure 14 - Gate charge test circuit

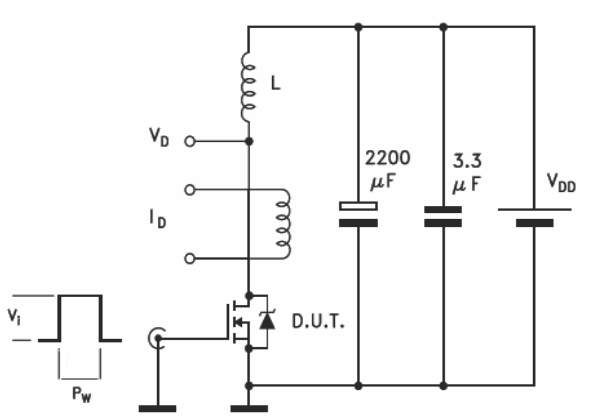


Figure 15- Unclamped Inductive load test circuit

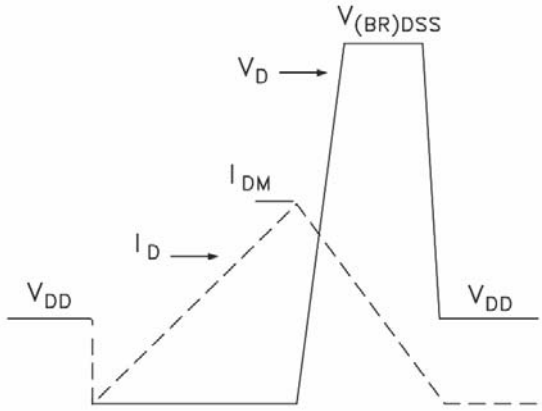


Figure 16 - Unclamped Inductive waveform

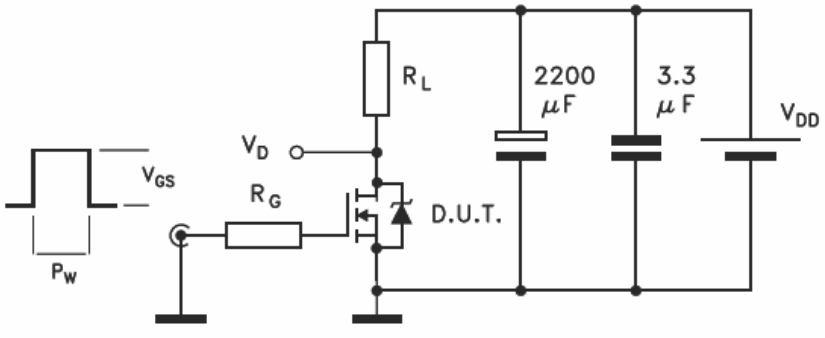
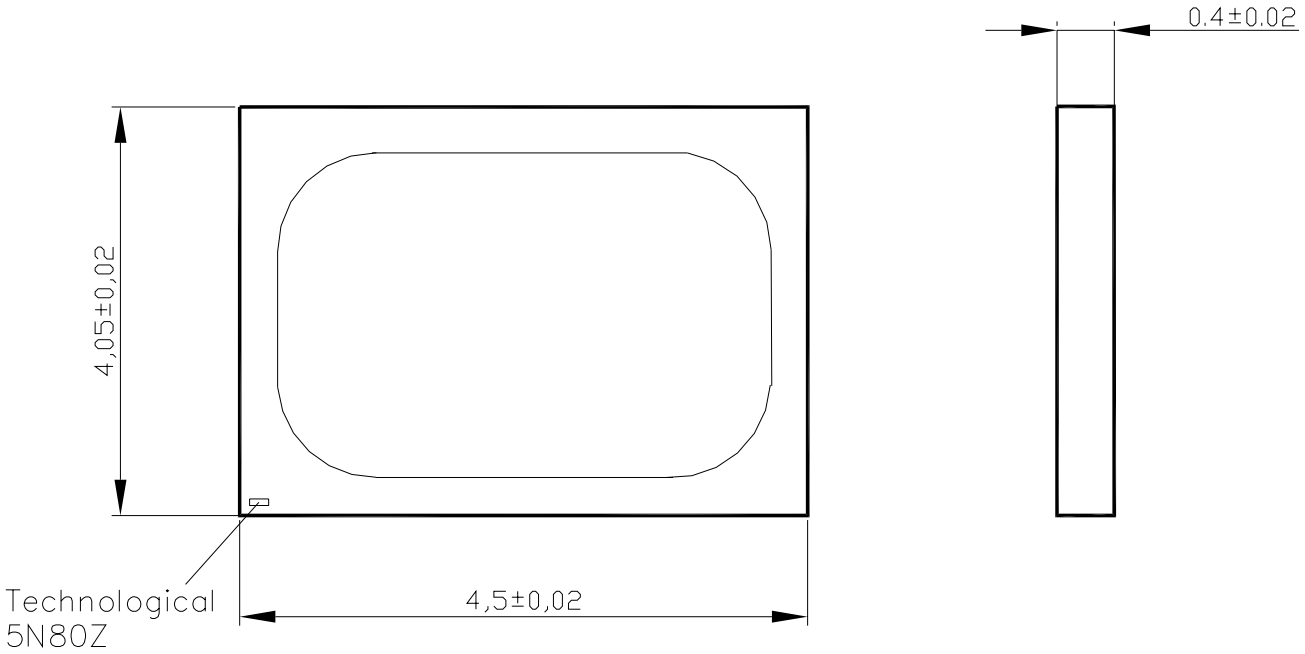


Figure 17 - Switching times test circuit for resistive load

Chip size



Package Dimensions TO-220 AB/3