HIGH-VOLTAGE LED DRIVER WITH BUILT-IN MOSFET SWITCH

IZ9921, IZ9922, IZ9923 are high-voltage LED driver control ICs with built-in MOSFET switch and intended for LED lighting control. They allow efficient operation of LED strings from voltage sources ranging up to 400VDC. The IZ9921/22 includes an internal high-voltage switching MOSFET controlled with fixed off-time T_{OFF} of approximately 10µs. The LED string is driven at constant current, thus providing constant light output and enhanced reliability. The output current is internally fixed at 20mA for IZ9921, 50mA for IZ9922 and 30mA for IZ9923. The peak current control scheme provides good regulation of the output current throughout the universal AC line voltage range of 85 to 264VAC or DC input voltage of 20 to 400V.

Main features:

- Operating temperature range -40 … +85 ºC;
- ON-resistance of the MOSFET switch 210 Ohm;
- OFF-state breakdown voltage of the MOSFET switch not less 500 V;
- ESD level 500V

Table 1 – Contact pad description

Contact pad number	Symbol	Description
01	TST	Test pad
02	PR3	Test pad
03	PR2	Test pad
04	TR	Test pad
05	PR1	Test pad
06	PR4	Test pad
07	U_{DD}	Supply voltage pad
08	TU	Test pad
09	GND	Ground
10	PU1	Test pad
11	PU2	Test pad
12	PU3	Test pad
13	DRAIN	MOSFET switch drain pad
14	GND	Ground

Note –

1 Contact pad 01 - 06, 08, 10, 11, 12, 14 (test pads) are used for testing process on manufacturing fab only (have not to be bonded by customer).

2 Contact pad 09, 14 (Ground) are electrically connected

Functional Block Diagram

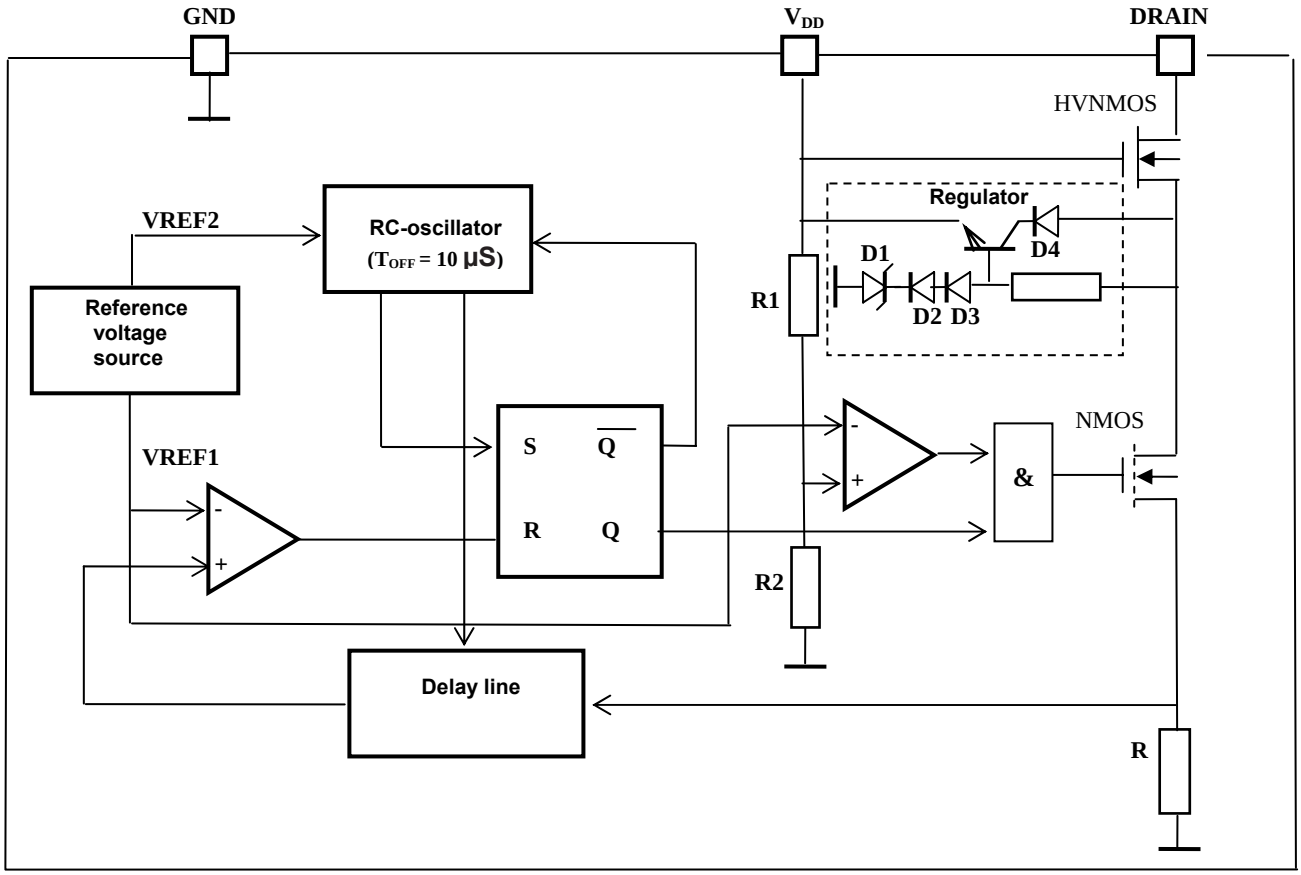


Fig 1 – Block diagram

Table 1 – Recommended operation conditions

Symbol	Parameter	Min	Max	Unit
V_{DRAIN}	Input voltage	20	400	V

Table 2 – Absolute maximum rating

Symbol	Parameter	Min	Max	Unit
V_{DRAIN}	Input voltage	-0,3	420	V
V_{DD}	Low-voltage part supply voltage	-0,3	10	V

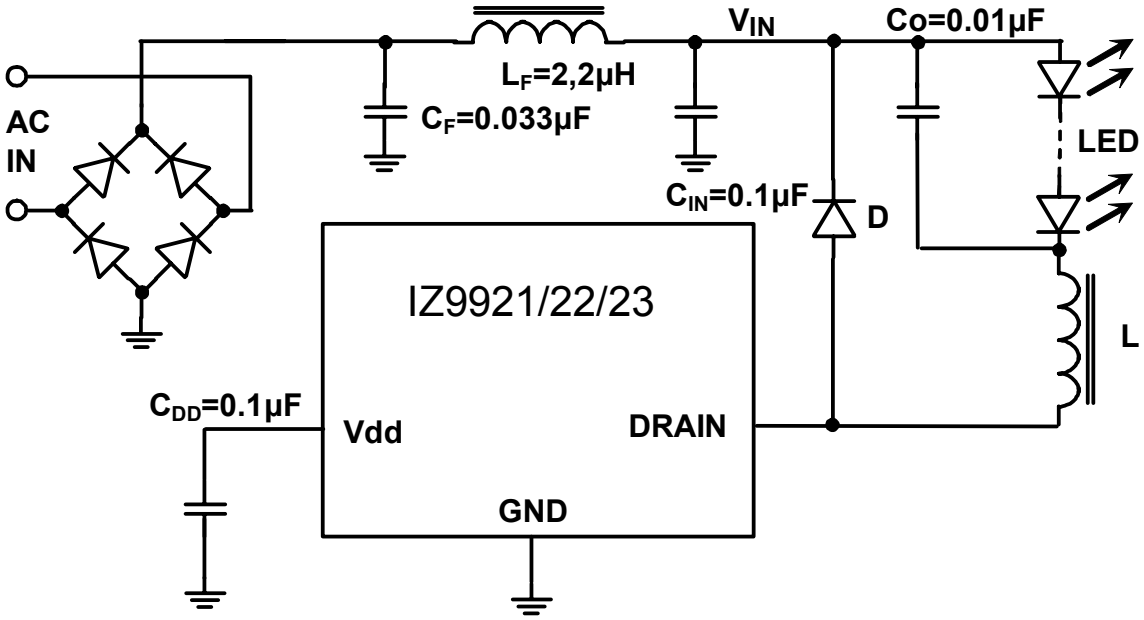
Table 3 – Electric parameters

Symbol	Parameter	Test condition	Min	Max	Ambient temperature, ºC	Unit
V_{DDR}	Regulator output voltage	V_{IN} = (20- 400)V	5,5	9,0	25 ± 10	V
I_{DD}	Low-voltage (control) part of IC consumptioncurrent	V_{DD} = 9,5 V V_{DRAIN} = 40 V	-	350		µA
R_{ON}	ON-resistance of the switch (DRAIN)	$V_{DD} = U_{DDR}$ I_{DRAIN} = 20 mA	-	210		Ohm
V_{UVLO}	Undervoltage threshold (Low-voltage part of IC)	$V_{DD} = U_{UVLO}$ I_{DRAIN} = 20 mA(IZ9921) I_{DRAIN} = 50 mA(IZ9922) I_{DRAIN} = 30 mA(IZ9923)	4,0	V_{DDR} – 0,3		V
I_{SAT}	MOSFET saturation current (DRAIN pin)	V_{DD}= V_{DDR} V_{SAT} = 50 V	100	-		mA
V_{BR}	MOSFET switch breakdown voltage	$V_{DD} = V_{DDR}$ I_{DRAIN} = 1 mA	500	-		V
I_{TH}	Threshold current IZ9921 IZ9922 IZ9923	$V_{DD} = V_{DDR}$	 20,5 52,0 30,8	 25,5 63,0 38,2	25 ± 10 -40 85	mA
T_{OFF}	OFF time (DRAIN)	$V_{DD} = V_{DDR}$	8,0	13,0	25 ± 10	µs
T_{ON}	Minimun ON-time of the switch (DRAIN)		-	650		ns
T_{BLANK}	Leading Edge Blanking Delay		200	400		ns

Functional Description

The IZ9921/22/23 are PWM peak current controllers for controlling a buck converter topology in continuous conduction mode (CCM). The output current is internally preset at 20mA (IZ9921), 50mA (IZ9922), or 30mA (IZ9923). When the input voltage of 20 to 400V appears at the DRAIN pin, the internal high-voltage linear regulator seeks to maintain a voltage of 7VDC at the VDD pin. Until this voltage exceeds the internally programmed under-voltage threshold, the output DRAIN is non-conductive. When the threshold is exceeded, the DRAIN turns on. The input current begins to flow into the DRAIN pin. Hysteresis is provided in the under-voltage comparator to prevent oscillation. When the input current exceeds the internal preset level, a current sense comparator resets an RS flip-flop, and the DRAIN turns off. At the same time, a one-shot circuit is activated that determines the duration of the off-state (10 µS typ.). As soon as this time is over, the flip-fl op sets again. The new switching cycle begins. A “blanking” delay of 300nS is provided that prevents false triggering of the current sense comparator due to the leading edge spike caused by circuit parasitics.

Typical Application Circuit



Selecting L and D

There is a certain trade-off to be considered between optimal sizing of the output inductor L and the tolerated output current ripple. The required value of L is inversely proportional to the ripple current dI_O in it.

$$L = \frac{T_{OFF\_MIAX} * V_O}{dI_O} \qquad (1)$$

V_O is the forward voltage of the LED string. T_{OFF} is the off time of the IZ9921/22/23. The output current in the LED string (I_O) is calculated then as:

$$I_O = I_{TH} - \frac{1}{2} dI_O \qquad (2)$$

where I_{TH} is the current sense comparator threshold.

The ripple current introduces a peak-to-average error in the output current setting that needs to be accounted for. Due to the constant off-time control technique used in theIZ9921/22/23, the ripple current is independent of the input AC or DC line voltage variation. Therefore, the output

current will remain unaffected by the varying input voltage. Adding a filter capacitor across the LED string can reduce the output current ripple even further, thus permitting a reduced value of L. However, one must keep in mind that the peak-to-average current error is affected by the variation of T_{OFF}. Therefore, the initial output current accuracy might be sacrificed at large ripple current in L.

Another important aspect of designing an LED driver with the IZ9921/22/23 is related to certain parasitic elements of the circuit, including distributed coil capacitance of L, junction capacitance and reverse recovery of the rectifier diode D, capacitance of the printed circuit board traces C_{PCB} and output capacitance C_{DRAIN} of the controller itself. These parasitic elements affect the efficiency of the switching converter and could potentially cause false triggering of the current sense comparator if not properly managed. Minimizing these parasitics is essential for efficient and reliable operation of the IZ9921/22/23. Coil capacitance of inductors is typically provided in the manufacturer's data books either directly or in terms of the self-resonant frequency (SRF).

$$SRF = 1/(2\pi\sqrt{LC_L}) \qquad (3)$$

where L is the inductance value, and C_L is the coil capacitance.

Charging and discharging this capacitance every switching cycle causes high-current spikes in the LED string. Therefore, connecting a small capacitor C_O (~10nF) is recommended to bypass these spikes. Using an ultra-fast rectifier diode for D is recommended to achieve high efficiency and reduce the risk of false triggering of the current sense comparator. Using diodes with shorter reverse recovery time t_{RR} and lower junction capacitance C_J achieves better performance. The reverse voltage rating V_R of the diode must be greater than the maximum input voltage of the LED lamp. The total parasitic capacitance present at the DRAIN pin of the IZ9921/22/23 can be calculated as:

$$C_P = C_{DRAIN} + C_{PCB} + C_L + C_J \qquad (4)$$

where and C_{DRAIN} is the DRAIN capacitance (C_{DRAIN} < 5pF), and C_{PSB} is the printed-circuit board capacitance.

When the switching MOSFET turns on, the capacitance C_P is discharged into the DRAIN pin of the IC. The discharge current is limited to about 150mA typically. However, it may become lower at increased junction temperature. The duration of the leading edge current spike can be estimated as:

$$T_{SPIKE} = t_{RR} + \frac{V_{IN} * C_P}{I_{SAT}} \qquad (5)$$

In order to avoid false triggering of the current sense comparator, C_P must be minimized in accordance with the following expression:

$$C_P < \frac{I_{SAT} * (T_{BLANK\_MIN} - t_{RR})}{V_{IN\_MAX}} \qquad (6)$$

where T_{BLANK_MIN} is the minimum blanking time of 200ns, and V_{IN_MAX} is the maximum instantaneous input voltage.

Estimating Power Loss

Discharging the parasitic capacitance C_P into the DRAIN pin of the IZ9921/22/23 is responsible for the bulk of the switching power loss. It can be estimated using the following equation:

$$P_{SWITCH} = \left(\frac{V_{IN}^2 * C_P}{2} + V_{IN} * I_{SAT} * t_{RR} \right) * F_S \qquad (7)$$

where Fs is the switching frequency, I_{SAT} is the saturated DRAIN current of the IZ921/22/23. The switching loss is the greatest at the maximum input voltage. The switching frequency is given by the following:

$$F_S \approx \frac{V_{IN} - V_O}{V_{IN} * T_{OFF}} \quad (8)$$

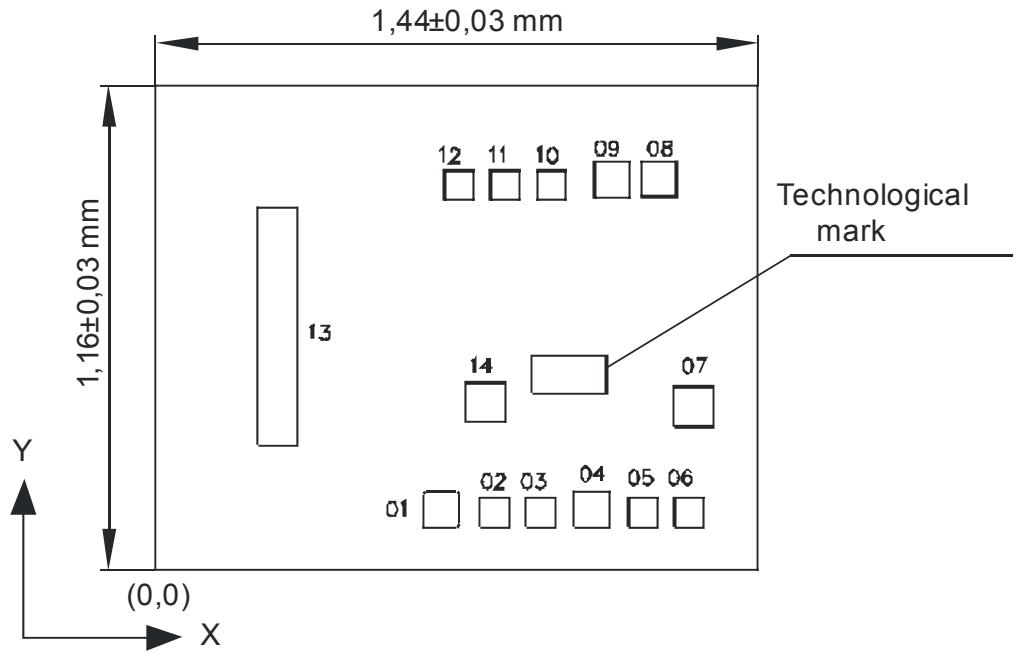
The switching power loss associated with turn-off transitions of the DRAIN pin can be disregarded. Due to the large amount of parasitic capacitance connected to this switching node, the turn-off transition occurs essentially at zero-voltage. Conduction power loss in the IZ9921/22/23 can be calculated as:

$$P_{COND} \approx I_O{}^2 * R_{ON} * \frac{V_O}{V_{IN}} + I_{DD} * (V_{IN} - V_O) \quad (9)$$

where R_{ON} is the ON resistance, I_{DD} is the internal linear regulator current.

$$P_{TOTAL} = P_{SWITCH} + P_{COND} \quad (10)$$

Contact pad layout diagram



Die thichness 0,46±0,02 mm.
Technological mark coordinates, um: x=898, y=424.

Table 5 – Technological mark

Type of IC	Technological mark
IZ9921	9921
IZ9922	9922
IZ9923	9923

Table 6 - Contact pad coordinates and sizes

Contact pad number	Coordinates (left bottom corner), um		Contact pad dimension, um
	X	Y	
01	639,5	103,5	85 x 85
02	775	103,5	70 x 70
03	885	103,5	70 x 70
04	999,5	103,5	85 x 85
05	1130	103,5	70 x 70
06	1240	103,5	70 x 70
07	1237,5	343,5	95 x 95
08	1160	894	85 x 85
09	1025,5	894	85 x 85
10	910,5	886	70 x 70
11	800,5	886	70 x 70
12	690,5	886	70 x 70
13	242,5	298,5	95 x 570
14	740,5	354	95 x 95
Note - Contact pad coordinates and dimensions are indicated under “Passivation” layer			