LCD DRIVER

The IZ602 is universal LCD controller designed to drive LCD with image element up to 128 (32x4). Instruction set makes IZ602 universal and suitable for applications with different types of displays. The circuit has 3-wire interface for communication with the host controller and the IZ602. Power down mode allow to reduce power consumption.

Main features:

- Operating voltage range: 2,4 V ~ 5,5V
- Built-in 256 kHz RC oscillator
- External 32,768 kHz crystal or 256 kHz frequency source input
- Selection of 1/2 or 1/3 bias
- Selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Number of driven columns up to 32
- Software setting of power down mode
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 8 modes of timer/WDT
- 32x4 LCD driver
- Built-in 32x4 bit display RAM
- 3-wire serial interface
- Programming of the operation modes
- Instruction set support operation and data exchange modes
- R/W address auto increment
- Three data accessing modes
- V_{LCD} pin allow to set LCD supply operating voltage

Table 1 – Pad description

Pad No	Pad Name	Function
01	$\overline{CS}$	Chip selection input
02	$\overline{RD}$	READ clock input
03	$\overline{WR}$	WRITE clock input
04	DATA	Serial data input/output
05	GND	Common
06	OSCO	Oscilator output
07	OSCI	Oscilator input
08	V_{LCD}	LCD power supply input
09	V_{DD}	Power supply input
10	$\overline{IRQ}$	Timer interruption output
11	BZ	Tone frequency output
12	$\overline{BZ}$	Tone frequency output
13	COM0	LCD common outputs
14	COM1	LCD common outputs
15	COM2	LCD common outputs
16	COM3	LCD common outputs
17	SEG32	LCD segment outputs
18	SEG31	LCD segment outputs

Table 1 continued

Pad No	Pad Name	Function
19	SEG30	LCD segment outputs
20	SEG29	LCD segment outputs
21	SEG28	LCD segment outputs
22	SEG27	LCD segment outputs
23	SEG26	LCD segment outputs
24	SEG25	LCD segment outputs
25	SEG24	LCD segment outputs
26	SEG23	LCD segment outputs
27	SEG22	LCD segment outputs
28	SEG21	LCD segment outputs
29	SEG20	LCD segment outputs
30	SEG19	LCD segment outputs
31	SEG18	LCD segment outputs
32	SEG17	LCD segment outputs
33	SEG16	LCD segment outputs
34	SEG15	LCD segment outputs
35	SEG14	LCD segment outputs
36	SEG13	LCD segment outputs
37	SEG12	LCD segment outputs
38	SEG11	LCD segment outputs
39	SEG10	LCD segment outputs
40	SEG9	LCD segment outputs
41	SEG8	LCD segment outputs
42	SEG7	LCD segment outputs
43	SEG6	LCD segment outputs
44	SEG5	LCD segment outputs
45	SEG4	LCD segment outputs
46	SEG3	LCD segment outputs
47	SEG2	LCD segment outputs
48	SEG1	LCD segment outputs

Chip structure

IZ602 integrates following units :
- circuit of control and timing interface
- built-in RC & crystal oscilators
- watchdog timer and time base generator
- 32x4 bit display RAM
- column and segment drivers
- bias circuit (LCD control levels former).

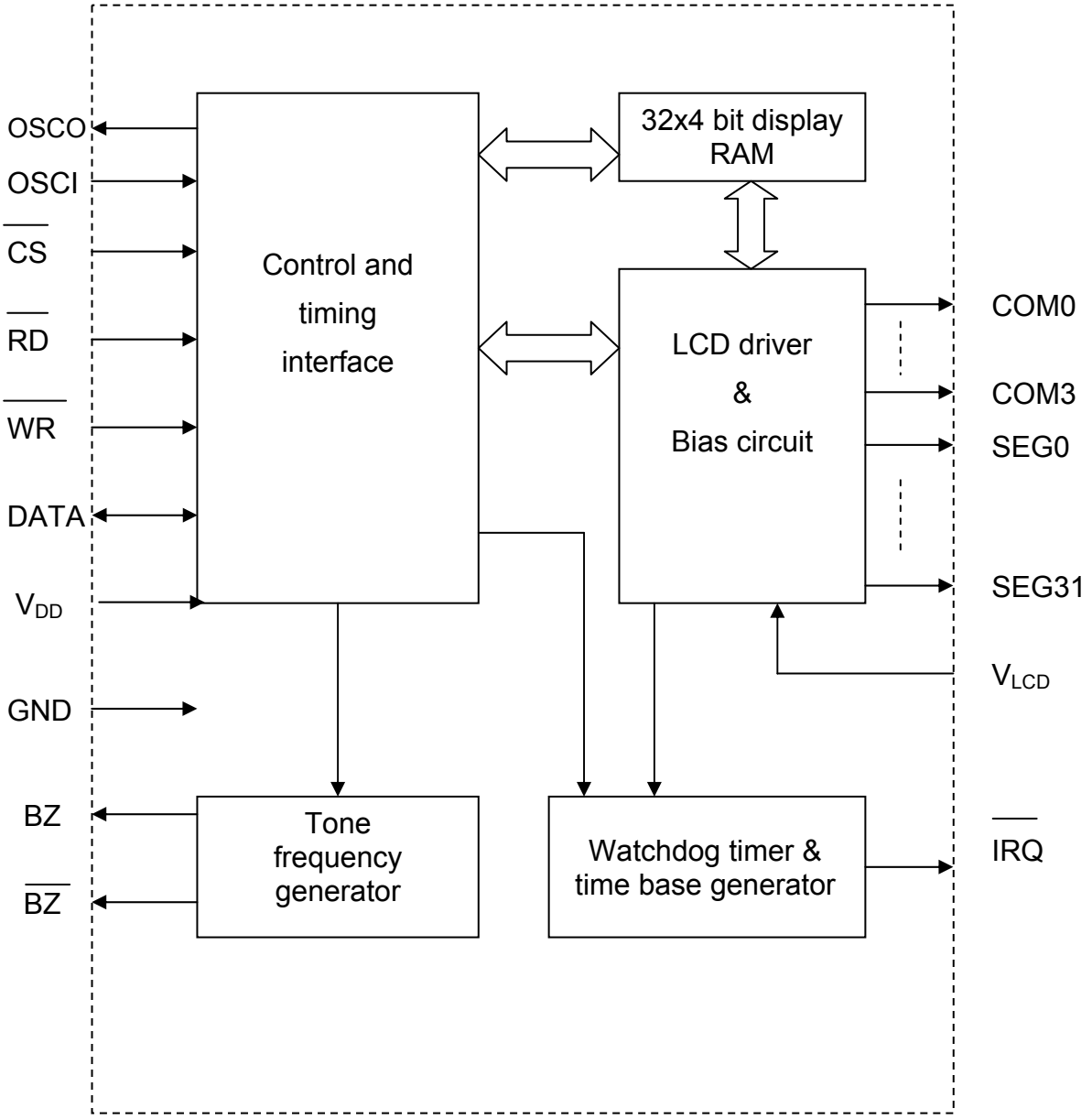


Fig 1 - IZ602 block diagram

Table 2 – Maximun ratings and recommended operation modes

Symbol	Parameters, units	Recommended operation mode		Maximum rating	
		Min.	Max.	Min.	Max.
U_{DD}	Supply voltage, V	2,4	5,5	- 0,3	5,6
U_{LCD}	LCD supply voltages, V	2,4	U_{DD}	- 0,3	5,6
U_{IH}	Input high voltages, V - Inputs DATA, $\overline{WR}$, $\overline{RD}$, $\overline{CS}$	0,8 U_{DD}	U_{DD}	-	U_{DD} + 0,3
U_{IL}	Input low voltages, V - Inputs DATA, $\overline{WR}$, $\overline{RD}$, $\overline{CS}$	0	0,2 U_{DD}	- 0,3	-
T_A	Ambient temperature, °C	- 60	125	- 45	85
T_J	Operating junction temperature, °C	- 60	125	- 45	85
T_{stg}	Storage temperature, °C	- 60	125	-	-

Table 4 – Electric parameters (T_A = 25 ºC)

Parameters, units	Symbol	Measurement mode	Targets	
			Min.	Max.
RC-oscilator operation consumption current, μA	I_{DD1}	U_{DD} = 3,0 V	-	300
		U_{DD} = 5,5 V	-	600
Crystal oscilator operation consumption current, μA	I_{DD2}	U_{DD} = 3,0 V	-	120
		U_{DD} = 5,5 V	-	240
External oscilator operation consumption current, μA	I_{DD3}	U_{DD} = 3,0 V	-	200
		U_{DD} = 5,5 V	-	400
Standby mode consumption current, μA	I_{STB}	U_{DD} = 3,0 V	-	5
		U_{DD} = 5,5 V	-	10
Output low current, mA outputs: DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$,	I_{OL1}	U_{DD} = 3,0 V U_{OL} = 0,3 V	0,5	-
		U_{DD} = 5,0 V U_{OL} = 0,5 V	1,3	-
Output high current, mA outputs: DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	I_{OH1}	U_{DD} = 3,0 V U_{OH} = 2,7 V	| - 0,4 |	-
		U_{DD} = 5,0 V U_{OH} = 4,5 V	| - 0,9 |	-
Output low current, μA outputs: COM0 - COM3	I_{OL2}	U_{DD} = 3,0 V U_{OL} = 0,3 V	80	-
		U_{DD} = 5,0 V U_{OL} = 0,5 V	150	-
Output high current, μA outputs: COM0 - COM3	I_{OH2}	U_{DD} = 3,0 V U_{OH} = 2,7 V	| - 80 |	-
		U_{DD} = 5,0 V U_{OH} = 4,5 V	| - 120 |	-
Output low current, μA outputs SEG1 - SEG32	I_{OL3}	U_{DD} = 3,0 V U_{OL} = 0,3 V	60	-
		U_{DD} = 5,0 V U_{OL} = 0,5 V	120	-
Output low current, μA outputs: SEG1 – SEG32	I_{OH3}	U_{DD} = 3,0 V U_{OH} = 2,7 V	| - 40 |	-
		U_{DD} = 5,0 V U_{OH} = 4,5 V	| - 70 |	-
Pull-high resistor on outputs : DATA, $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, kΩ	R_{PH1}	U_{DD} = 3,0 V	40	150
	R_{PH2}	U_{DD} = 5,0 V	30	100
Note - U_{LCD} has to be set equal to U_{dd} for all modes				

Table 5 – Switching parameters

Parameter, unit	Symbol	Measurement mode	Target		
			Min.	Typ.	Max.
External oscilator clock frequency, kHz	f_{SYS1}	U_{DD} = 2,4 V	-	256	-
		U_{DD} = 5,5 V	-	256	-
Crystal oscilator clock frequency, kHz	f_{SYS2}	U_{DD} = 2,4 V	-	32,768	-
		U_{DD} = 5,5 V	-	32,768	-
RC - oscilator clock frequency, kHz	f_{SYS3}	U_{DD} = 2,4 V	-	256	-
		U_{DD} = 5,5 V	-	256	-
LCD drive signal interval, s	T_{COM}	RC - oscilator	-	(1024*N)/f_{SYS3}	-
		Crystal oscilator	-	(128*N)/ f_{SYS2}	-
		External oscilator	-	(1024*N)/f_{SYS1}	-
$\overline{WR}$ clock frequency, kHz	f_{CLK1}	U_{DD} = 3,0 V Porosity 50%	-	-	150
		U_{DD} = 5,5 V Porosity 50%	-	-	300
$\overline{RD}$ clock frequency, kHz	f_{CLK2}	U_{DD} = 3,0 V Porosity 50%	-	-	75
		U_{DD} = 5,5 V Porosity 50%	-	-	150
Clock pulses $\overline{WR}$, $\overline{RD}$ width (Fig. 2), μs	t_{CLK}	U_{DD} = 3,0 V Write	3,34	-	-
		U_{DD} = 3,0 V Read	6,67	-	-
		U_{DD} = 5,5 V Write	1,67	-	-
		U_{DD} = 5,5 V Read	3,34	-	-
Rise/fall edge width of the clock pulses (Fig. 2), ns	t_r, t_f	U_{DD} = 3,0 V	-	-	120
		U_{DD} = 5,5 V	-	-	120
Setup Time for Data to $\overline{WR}$, $\overline{RD}$ clock pulse (Fig. 3), ns	t_{SU}	U_{DD} = 3,0 V	120	-	-
		U_{DD} = 5,5 V	120	-	-

Table 5 continued

Parameter, unit	Symbol	Measurement mode	Target		
			Min.	Typ.	Max.
Hold Time for Data to $\overline{WR}$, $\overline{RD}$ clock pulse (Fig.3),ns	t_h	U_{DD} = 3,0 V	120	-	-
		U_{DD} = 5,5 V	120	-	-
Serial Interface Reset Pulse Widht (Fig. 4), ns	t_{CS}	U_{DD} = 3,0 V	250	-	-
		U_{DD} = 5,5 V	250	-	-
Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Widht (Fig. 4), ns	t_{SU1}	U_{DD} = 3,0 V	120	-	-
		U_{DD} = 5,5 V	120	-	-
Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Widht (Fig. 3), ns	t_{h1}	U_{DD} = 3,0 V	100	-	-
		U_{DD} = 5,5 V	100	-	-

Notes

1. Clock frequency with RC-oscilator & clock frequency with crystal oscilator are controled by means measurement of the LCD driving signal interval at one of outputs COM3 – COM0 adjusted for division factor specified in the table.

2. N = (2 – 4) – specified multiplex

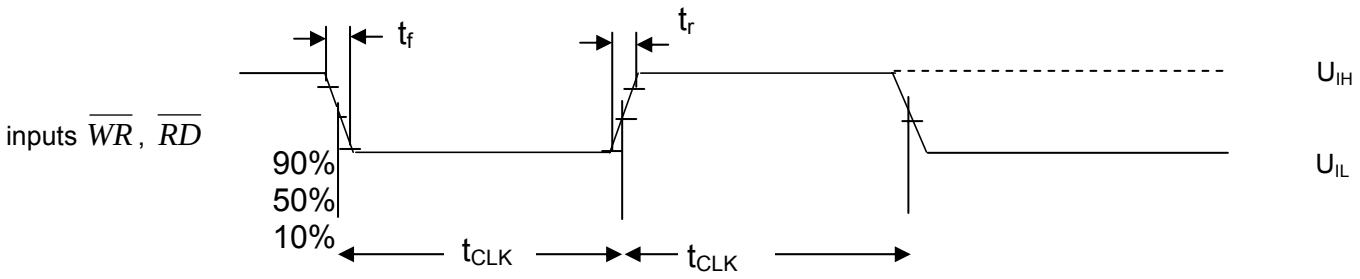


Fig. 2 – $\overline{WR}$, $\overline{RD}$ inputs timing diagram

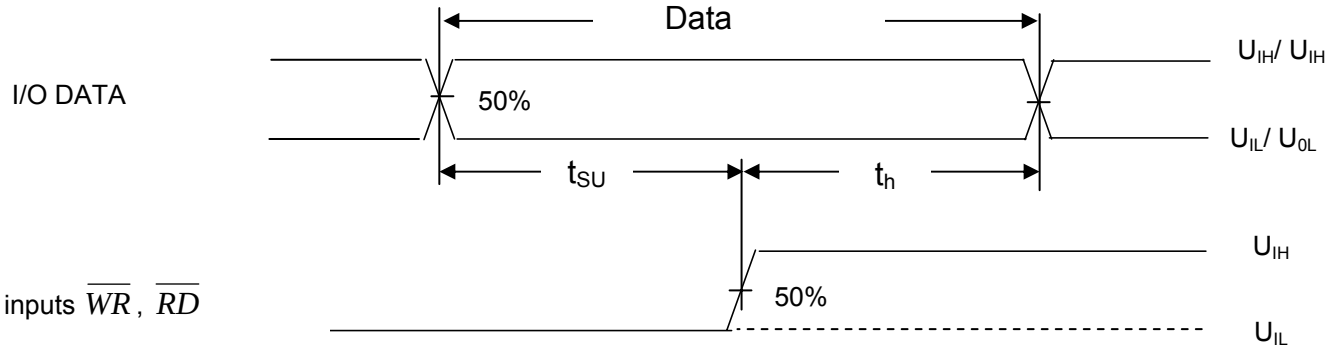


Fig. 3 – Read/write timing diagram

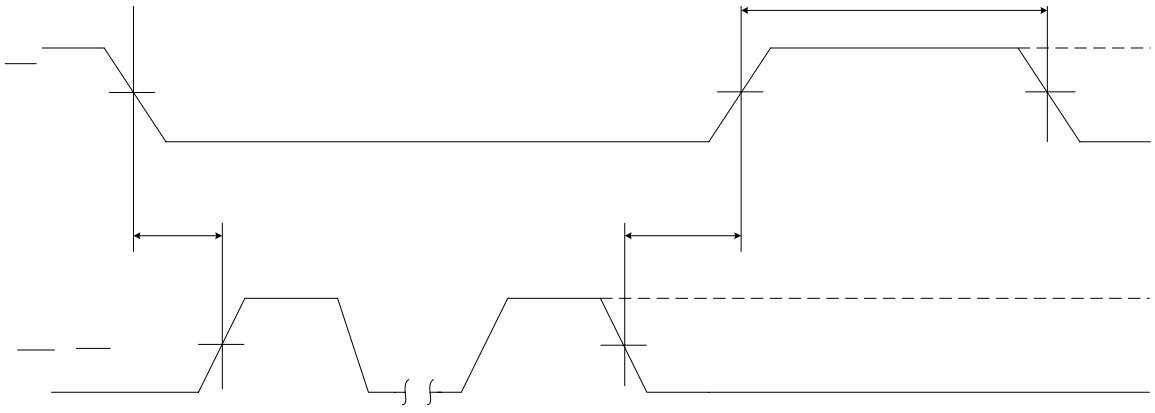
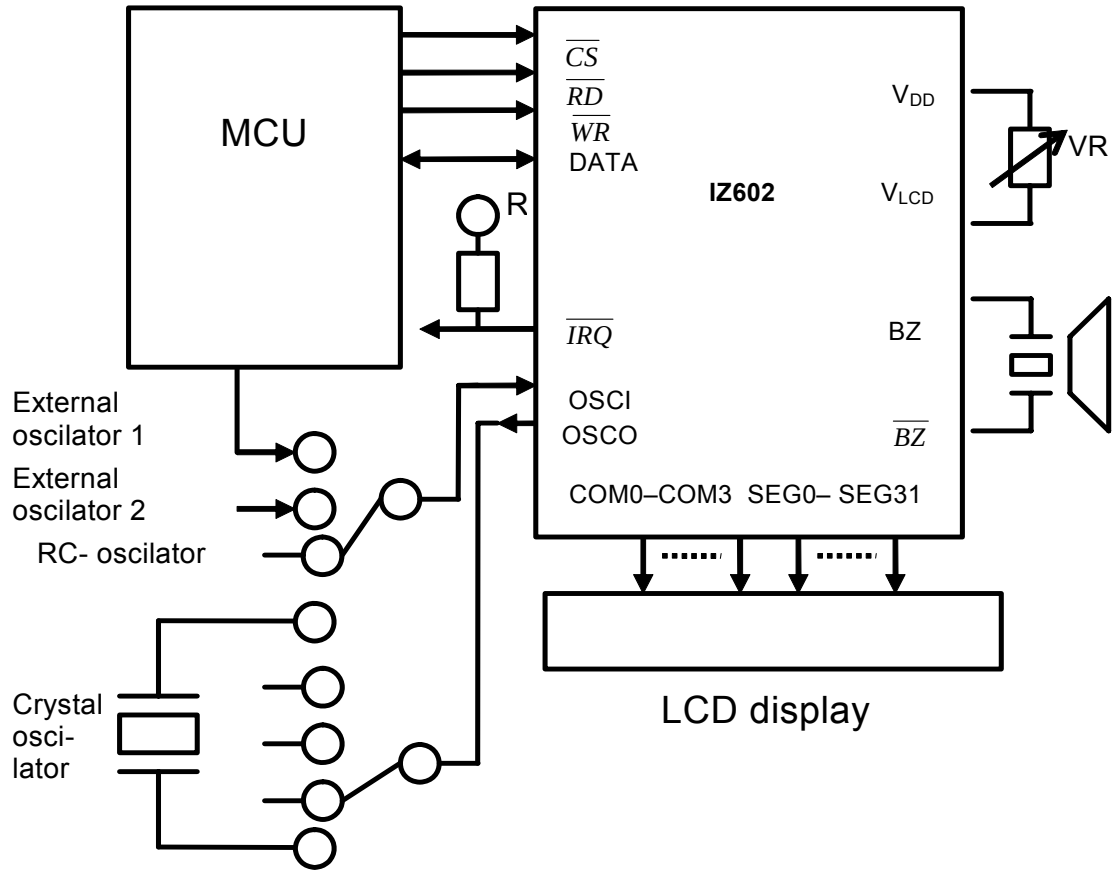


Fig. 4 – Chip select (CS input) timing diagram



Parameters of the crystal oscilator

Fp = 32768 Hz

C_L = 12,5 pF

C_1 = 0,004 pF

C_O = 2,5 pF

Rs = 35 kΩ

Q = 35000

Fig. 5 - IZ602 application diagram

Functional description

Built-in memory - Display RAM

The display RAM is organized into 32x4 bits and purposed for storage of the displayed data. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands.

	COM3	COM2	COM1	COM0	
SEG0					0
SEG1					1
SEG2					2
SEG3					3
⋮	⋮	⋮	⋮	⋮	⋮
SEG31					31
	D3	D2	D1	D0	Addr Data

Address 6 bit (A5, A4..,A0)

Data 4 bits (D3, D2, D1, D0)

Fig. 6 – RAM mapping

System oscillator

Base frequency 32768 Hz provides operation of the time base generator (further timer), Watchdog Timer (WDT), tone frequency generation and multiplex (DUTY).

There are three available sources of the clock for chip: on-chip RC oscillator (256 kHz), a crystal oscillator (32,768 kHz), or an external 256 kHz clock. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the timer/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using of the SYS DIS command reduces power consumption.

But if the external clock source is selected as the system clock, SYS DIS command cannot perform the oscillator turn off and activation of the power down mode.

The crystal oscillator option can be applied to connect an external frequency source of 32 kHz. In this case, the system fails to enter the power down mode, similar to the case in the external 256 kHz clock source operation. At the initial system power on, the IZ 602 is at the SYS DIS state.

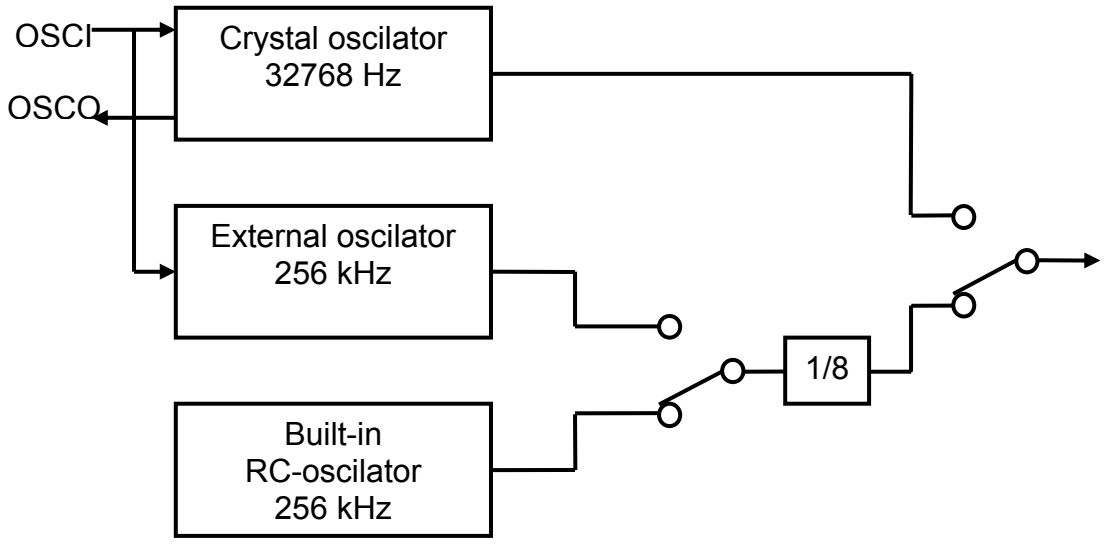


Fig. 7 – Base frequency forming

Time base and Watchdog Timer (WDT)

The time base generator is consist of an 8 - bit count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT) is composed of an 8-bit counter with a 2 - bit count-up counter, and is designed to interrupt the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT operation will result if an internal WDT flag is set by a command option. The outputs of the timer and of the WDT time-out flag can be connected to the $\overline{IRQ}$ output by a command option. There are totally eight frequency sources available for the timer and the WDT clock. The frequency is calculated by the following equation.

$$f_{WDT} = \frac{32kHz}{2^n} \; ; \qquad (1)$$

the value of n ranges from 0 to 7 by command options.

The 32 kHz in the equation (1) indicates that the source of the system frequency is derived from a crystal oscillator of 32,768 kHz, an on-chip oscillator (256 kHz), or an external frequency of 256 kHz. If an on-chip oscillator (256 kHz) or an external 256 kHz frequency is chosen as the source of the system frequency, the frequency source is prescaled to 32 kHz by a 3 - bit prescaler.

Commands of the timer (time base generator) and the WDT are related, since the time base generator and WDT share the same 8 – bit counter. For example, the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the $\overline{IRQ}$ pin). After the TIMER EN command is executed, the WDT is disconnected from the $\overline{IRQ}$ pin, and the output of the time base generator is connected to the $\overline{IRQ}$ pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator is

cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the $\overline{IRQ}$ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will stay at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued. After the $\overline{IRQ}$ output is disabled the $\overline{IRQ}$ pin will remain at the floating state. The $\overline{IRQ}$ output can be enabled or disabled by executing the $\overline{IRQ}$ EN or the $\overline{IRQ}$ DIS command, respectively. The $\overline{IRQ}$ EN makes the output of the time base generator or of the WDT time-out flag appear on the $\overline{IRQ}$ pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.

If an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the IZ602 will continue working until system power fails or the external clock source is removed. After the system power on, the $\overline{IRQ}$ will be disabled.

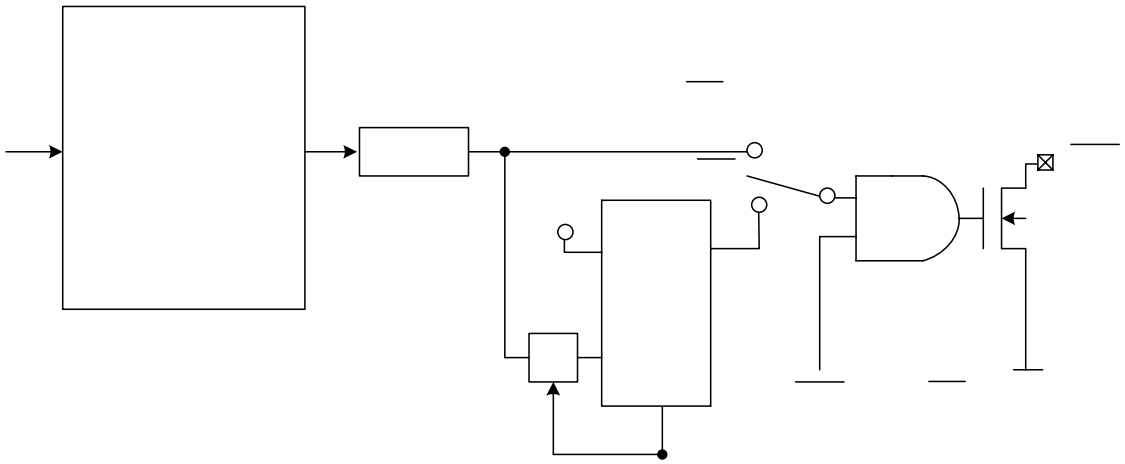


Fig. 8 - Configuration of the time base generator along with the WDT

Tone output

A simple tone generator is implemented in the IZ602. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone frequency to 4 kHz and 2 kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at low level.

LCD driver

The IZ602 is a LCD driver with serial interface

The bias 1/2 or 1/3 can be used with any level of the multiplex implemented on-chip for each bias. This feature makes the IZ602 suitable for different LCD applications. The LCD driving clock is derived from the system clock. The LCD OFF command disable the LCD bias generator and thus turns off the LCD display. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator.

The LCD corresponding commands are summarized in the table.5. Due to these the LCD related commands, the IZ602 can be compatible with most types of LCD panels.

Table 6 – LCD control instruction

Name	Command Code	Function
LCD OFF	**1 0 0** 0 0 0 0 0 0 1 0 X	Turn off LCD (outputs)
LCD ON	**1 0 0** 0 0 0 0 0 0 1 1 X	Turn on LCD (outputs)
BIAS & COM	**1 0 0** 0 0 1 0 a b X c X	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option

Command format

The operation mode can be configured by the software setting. There are two operation modes of the IZ602. The first applies to the use of chip resources, the second is used to transfer data displayed on the LCD screen. The mode of access to chip resouces is called the command mode.

In this mode, indicator of command is the code note 100, called the command ID. This ID is placed before the first command. This ID is omitted for second and followed commands. Command mode contains commands applying various features of the system, option of the source of base frequency, the LCD control commands, option of the tone frequency, command to set the timer, WDT and control commands. Data mode includes the operations READ, WRITE and READ-MODIFY-WRITE. Table 7 shows the ID to command mode and data mode. Full command set is presented in Table 8. Command or data mode ID must be set before the command or data is transferred. If first commaqnd followed by other, command mode ID 100 can be omitted. In the case where the system operates in an random command stream or in a data stream with inconsistent addresses, pin NCS has to be set to "1" (the previous mode is reset), then "0". After that, before performing a new operation, appropriate mode ID has to be set.

Interfacing

Four lines are required to interface with the IZ602. The $\overline{CS}$ line is used to initialize the serial interface and to terminate the communication between the host controller and the IZ602. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the IZ602 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the IZ602.

The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line.

The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal.

The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the IZ602 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the IZ602.

Table 7 – Command and data modes

Operation	Mode	Operation ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

Table 8 - IZ602 command set

Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SIS DIS	1 0 0	0000 – 0000 - X	C	Turn off both system oscillator and LCD bias generator	Yes
SIS EN	1 0 0	0000 – 0001 - X	C	Turn on system oscillator	
LCD OFF	1 0 0	0000 – 0010 - X	C	Turn off LCD bias generator	Yes
LCD ON	1 0 0	0000 – 0011 - X	C	Turn on LCD bias generator	
TIMER DIS	1 0 0	0000 – 0100 - X	C	Disable time base output	
WDT DIS	1 0 0	0000 – 0101 - X	C	Disable WDT time-out flag output	
TIMER EN	1 0 0	0000 – 0110 - X	C	Enable time base output	
WDT EN	1 0 0	0000 – 0111 - X	C	Enable WDT time-out flag output	
TONE OFF	1 0 0	0000 – 1000 - X	C	Turn off tone outputs	Yes
TONE ON	1 0 0	0000 – 1001 - X	C	Turn on tone outputs	
CLR TIMER	1 0 0	0000 - 11XX - X	C	Clear the contents of time base generator	
CLR WDT	1 0 0	0000 - 111X - X	C	Clear the contents of WDT stage	
XTAL 32K	1 0 0	0001 - 01XX - X	C	System clock source, crystal oscillator	
RC 256K	1 0 0	0001 - 10XX - X	C	System clock source, on-chip RC oscillator	Yes
EXT 256K	1 0 0	0001 - 11XX - X	C	System clock source, external clock source	
BIAS 1 / 2	1 0 0	0010 - abX0 - X	C	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
BIAS 1 / 3	1 0 0	0010 - abX1 - X	C	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 4K	1 0 0	010X – XXXX - X	C	Tone frequency, 4 kHz	
TONE 2K	1 0 0	011X – XXXX - X	C	Tone frequency, 2 kHz	
IRQ DIS	1 0 0	100X - 0XXX - X	C	Disable $\overline{\text{IRQ}}$ output	Yes

Table 8 continued

Name	ID	Command Code	D/C	Function	Def.
IRQ EN	1 0 0	100X - 1XXX - X	C	Enable $\overline{IRQ}$ output	
F1	1 0 0	101X - X000 - X	C	Time base/WDT clock output: 1 Hz The WDT time-out flag after: 4s	
F2	1 0 0	101X - X001 - X	C	Time base/WDT clock output: 2 Hz The WDT time-out flag after: 2s	
F4	1 0 0	101X - X010 - X	C	Time base/WDT clock output: 4 Hz The WDT time-out flag after: 1s	
F8	1 0 0	101X - X011 - X	C	Time base/WDT clock output: 8 Hz The WDT time-out flag after: 1/2 s	
F16	1 0 0	101X - X100 - X	C	Time base/WDT clock output: 16 Hz The WDT time-out flag after: 1/4 s	
F32	1 0 0	101X - X101 - X	C	Time base/WDT clock output: 32 Hz The WDT time-out flag after: 1/8 s	
F64	1 0 0	101X - X110 - X	C	Time base/WDT clock Output: 64 Hz The WDT time-out flag after: 1/16 s	
F128	1 0 0	101X - X111 - X	C	Time base/WDT clock output: 128 Hz The WDT time-out flag after: 1/32 s	Yes
TEST	1 0 0	1110 – 0000 - X	C	Test mode, user don't use	
NORMAL	1 0 0	1110 – 0011 - X	C	Normal mode	Yes

Note: X : Don`t care “0” or “1”
A5~A0 : RAM addresses
D3~D0 : RAM data
D/C : Data/command mode
ID – Operation code
Def. : Power on reset default

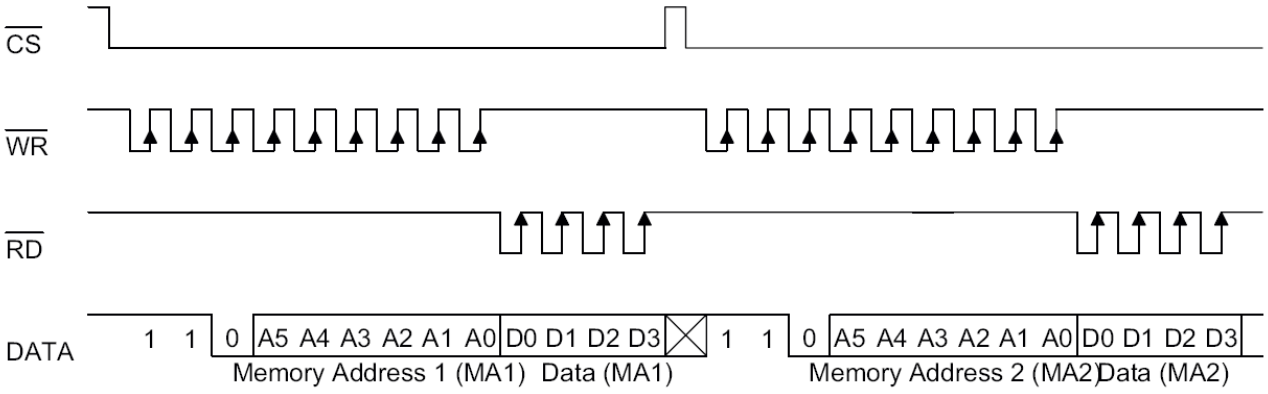


Fig.9 –READ operation (Command code: 1 1 0)

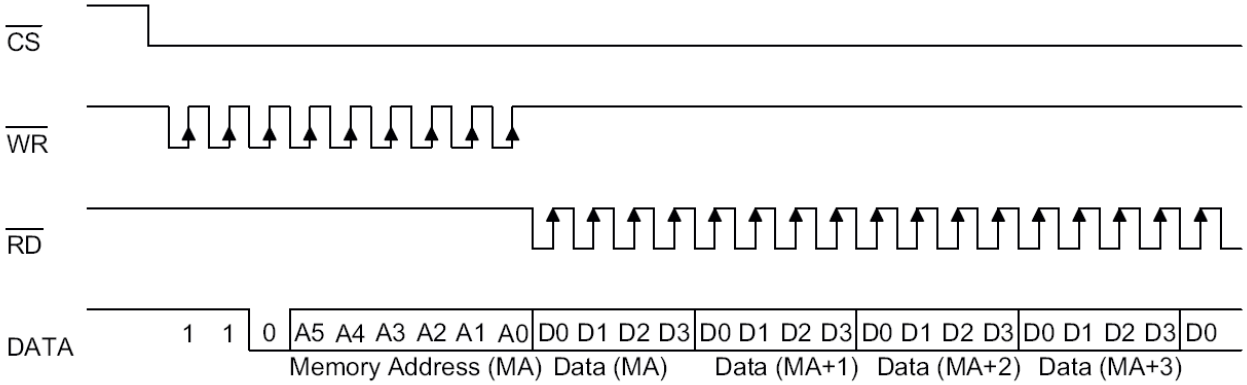


Fig. 10 –READ operation (successive address)

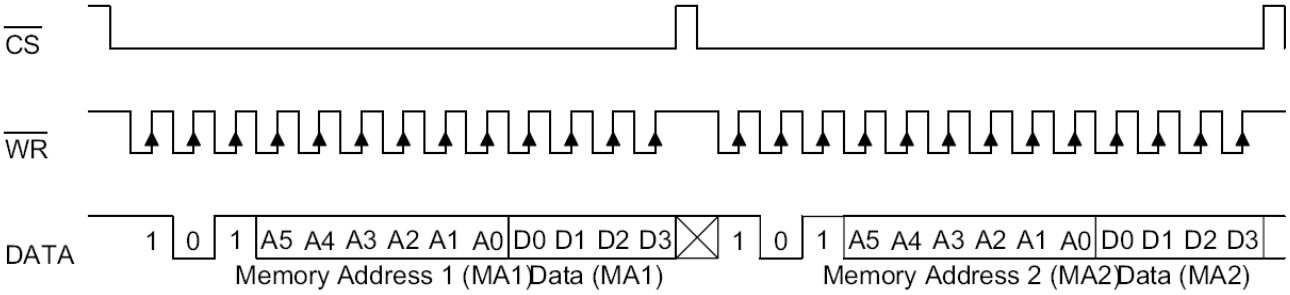


Fig. 11 –WRITE operation (Command code: 1 0 1)

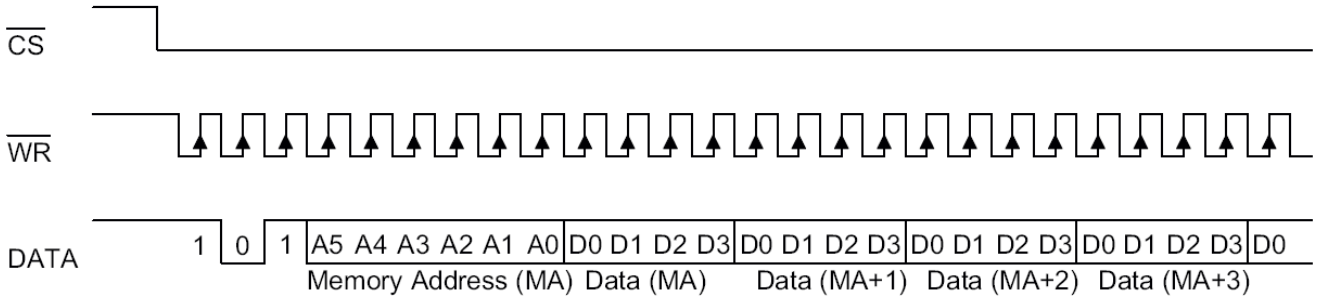


Fig. 12 –Write operation (writing of data with successive address)

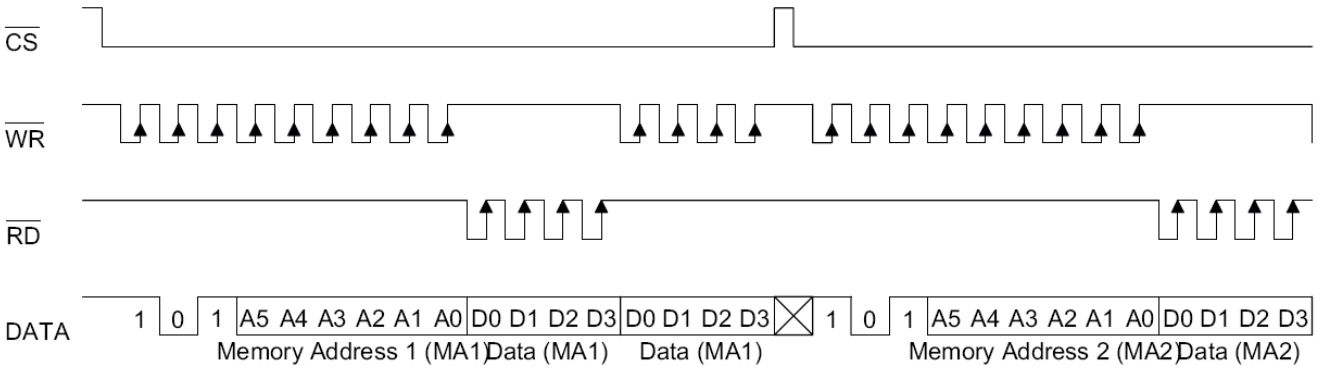


Fig. 13 –READ-MODIFY-WRITE operation (command code: 1 0 1)

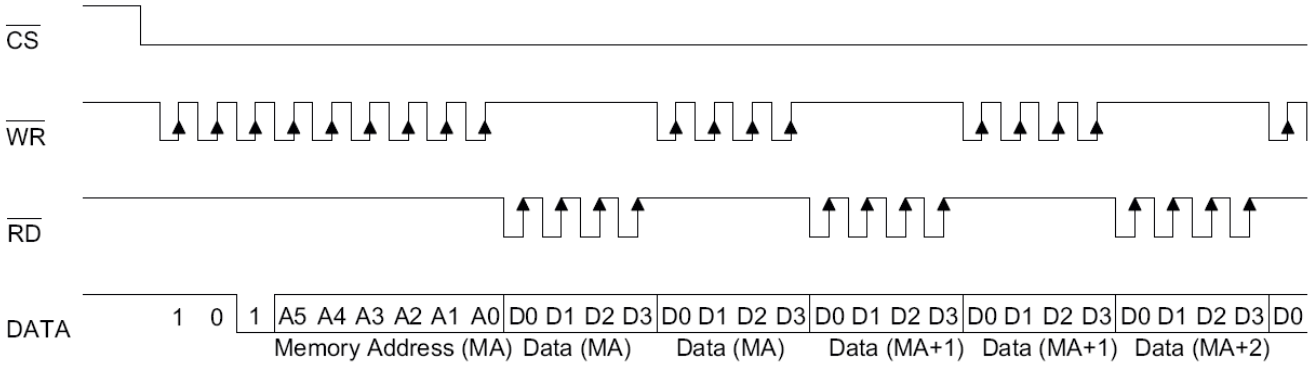


Fig.14 –READ-MODIFY-WRITE operation (successive address)

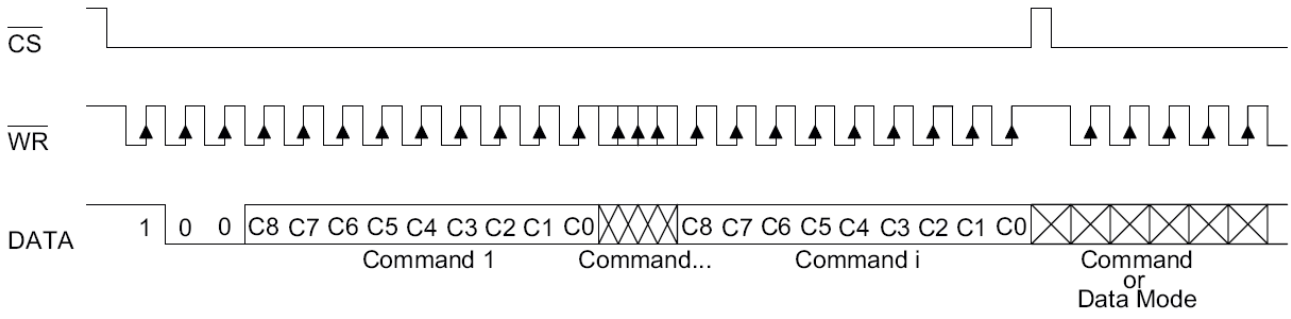


Fig. 15 – Command mode (Command code: 1 0 0)

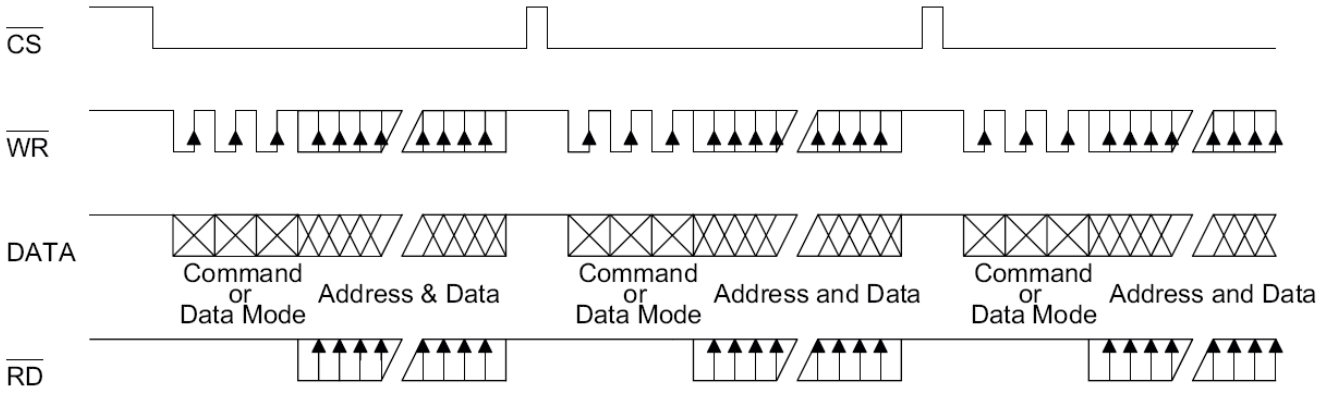
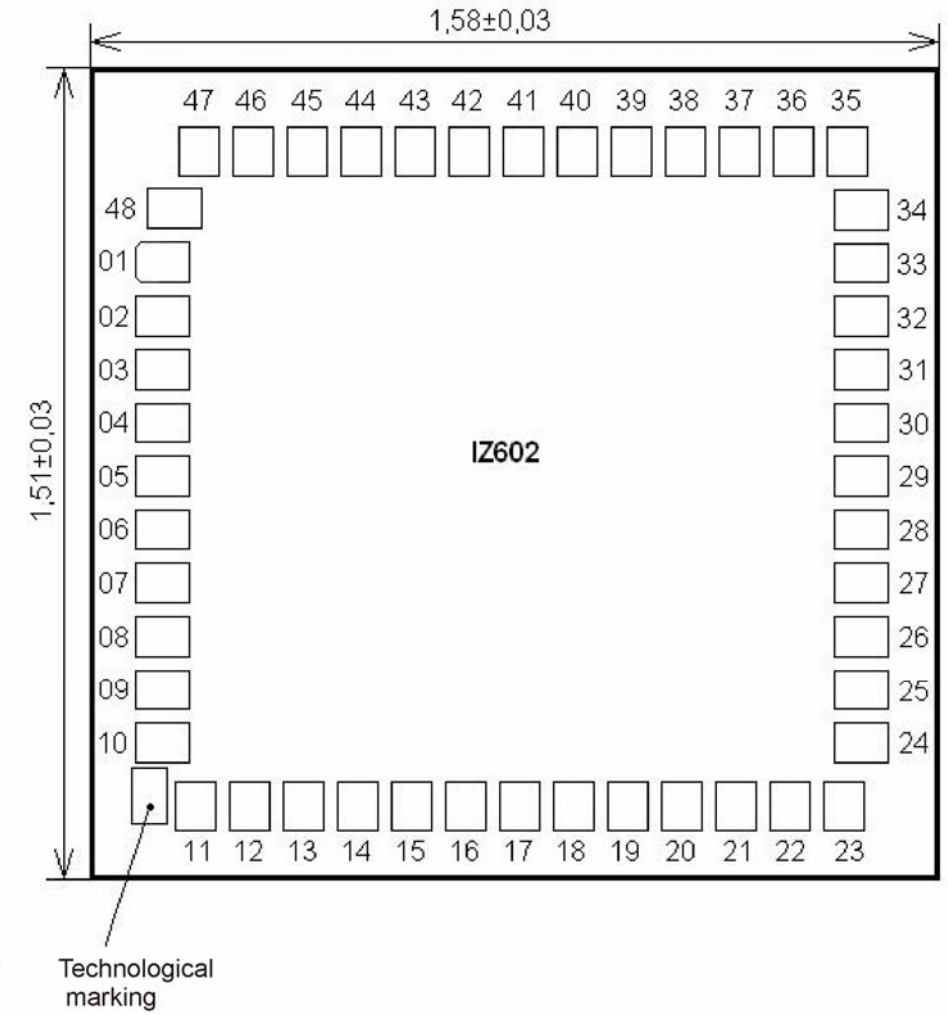


Fig. 16 – Data mode and command mode



Technological mark IZ602 coordinates (mm): left bottom corner. x = 0,094 , y = 0,105.

Fig. 17 – Chip layout diagram

Table 9 – Contact pad location

Contact pad number	Coordinates (ref. to left bottom corner), mm		Contact pad size, mm	Contact pad number	Coordinates (ref. to left bottom corner), mm		Contact pad size, mm
	X	Y			X	Y	
01	0,105	1,115	0,080 x 0,070	25	1,385	0,315	0,080 x 0,070
02	0,105	1,015	0,080 x 0,070	26	1,385	0,415	0,080 x 0,070
03	0,105	0,915	0,080 x 0,070	27	1,385	0,515	0,080 x 0,070
04	0,105	0,815	0,080 x 0,070	28	1,385	0,615	0,080 x 0,070
05	0,105	0,715	0,080 x 0,070	29	1,385	0,715	0,080 x 0,070
06	0,105	0,615	0,080 x 0,070	30	1,385	0,815	0,080 x 0,070
07	0,105	0,515	0,080 x 0,070	31	1,385	0,915	0,080 x 0,070
08	0,105	0,415	0,080 x 0,070	32	1,385	1,015	0,080 x 0,070
09	0,105	0,315	0,080 x 0,070	33	1,385	1,115	0,080 x 0,070
10	0,105	0,215	0,080 x 0,070	34	1,385	1,215	0,080 x 0,070
11	0,158	0,105	0,070 x 0,080	35	1,375	1,315	0,070 x 0,080
12	0,258	0,105	0,070 x 0,080	36	1,270	1,315	0,070 x 0,080
13	0,358	0,105	0,070 x 0,080	37	1,160	1,315	0,070 x 0,080
14	0,458	0,105	0,070 x 0,080	38	1,060	1,315	0,070 x 0,080
15	0,558	0,105	0,070 x 0,080	39	0,960	1,315	0,070 x 0,080
16	0,658	0,105	0,070 x 0,080	40	0,860	1,315	0,070 x 0,080
17	0,758	0,105	0,070 x 0,080	41	0,760	1,315	0,070 x 0,080
18	0,858	0,105	0,070 x 0,080	42	0,660	1,315	0,070 x 0,080
19	0,958	0,105	0,070 x 0,080	43	0,560	1,315	0,070 x 0,080
20	1,058	0,105	0,070 x 0,080	44	0,460	1,315	0,070 x 0,080
21	1,158	0,105	0,070 x 0,080	45	0,360	1,315	0,070 x 0,080
22	1,268	0,105	0,070 x 0,080	46	0,260	1,315	0,070 x 0,080
23	1,373	0,105	0,070 x 0,080	47	0,160	1,315	0,070 x 0,080
24	1,385	0,215	0,080 x 0,070	48	0,125	1,315	0,080 x 0,070
Note: Contact pad coordinates and size are indicated under «Passivation» layer							