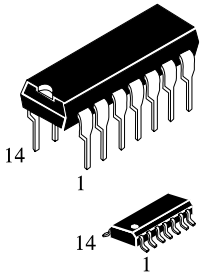
IN74HC14A

Hex Schmitt-Trigger Inverter



ORDERING INFORMATION

IN74HC14AN	Plastic
IN74HC14AD	SOIC
IZ74HC14A	Chip

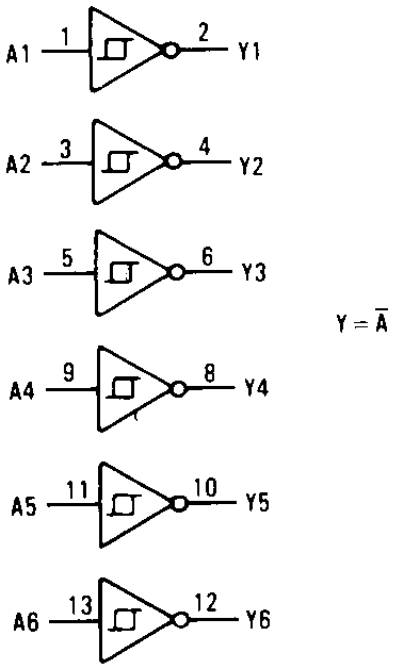
T_A = -55° to 125° C for all packages

The IN74HC14A is identical in pinout to the LS/ALS14. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

The IN74HC14A is useful to "square up" slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the IN74HC14A finds applications in noisy environments.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices

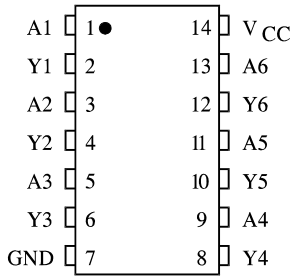
LOGIC DIAGRAM



$Y = \overline{A}$

PIN 14 =V_{CC}
PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs	Output
A	Y
L	H
H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r , t_f	Input Rise and Fall Time (Figure 1)	-	No Limit*	ns

* When V_{IN} ≈50% V_{CC} , I_{CC} > 1mA

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_T+max	Maximum Positive-Going Input Threshold Voltage	V_{OUT}=0.1 V $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_T+min	Minimum Positive-Going Input Threshold Voltage	V_{OUT}=0.1 V $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	1.0 2.3 3.0	0.95 2.25 2.95	0.95 2.25 2.95	V
V_T-max	Maximum Negative-Going Input Threshold Voltage	V_{OUT}=V_{CC} -0.1 V $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	0.9 2.0 2.6	0.95 2.05 2.65	0.95 2.05 2.65	V
V_T-min	Minimum Negative-Going Input Threshold Voltage	V_{OUT}=V_{CC}-0.1 V $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
$V_H$max *	Maximum Hysteresis Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	1.2 2.25 3.0	1.2 2.25 3.0	1.2 2.25 3.0	V
$V_H$min *	Minimum Hysteresis Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.5	0.2 0.4 0.5	0.2 0.4 0.5	0.2 0.4 0.5	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} \le V_T$-min $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN} \le V_T$-min $\|I_{OUT}\| \le 4mA$ $\|I_{OUT}\| \le 5.2mA$	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} \ge V_T$+max $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN} \ge V_T$+max $\|I_{OUT}\| \le 4mA$ $\|I_{OUT}\| \le 5.2mA$	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0μA	6.0	1.0	10	40	μA

* $V_H$min>(V_T+min)-(V_T-max); $V_H$max=(V_T+max)-(V_T-min)

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 4.5 6.0	95 19 16	120 24 20	145 29 25	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Per Inverter) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$		T_A=25°C,V_{CC}=5.0 V 22			pF

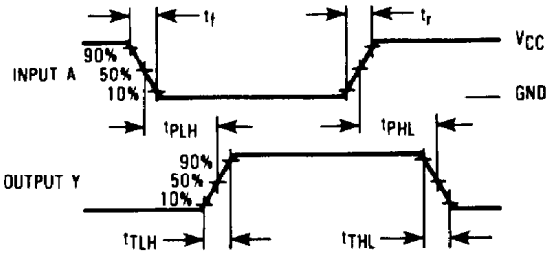


Figure 1. Switching Waveforms

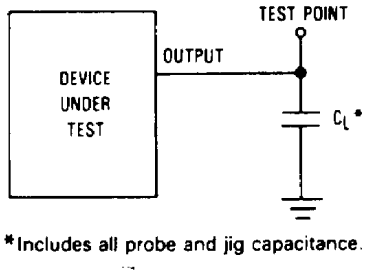
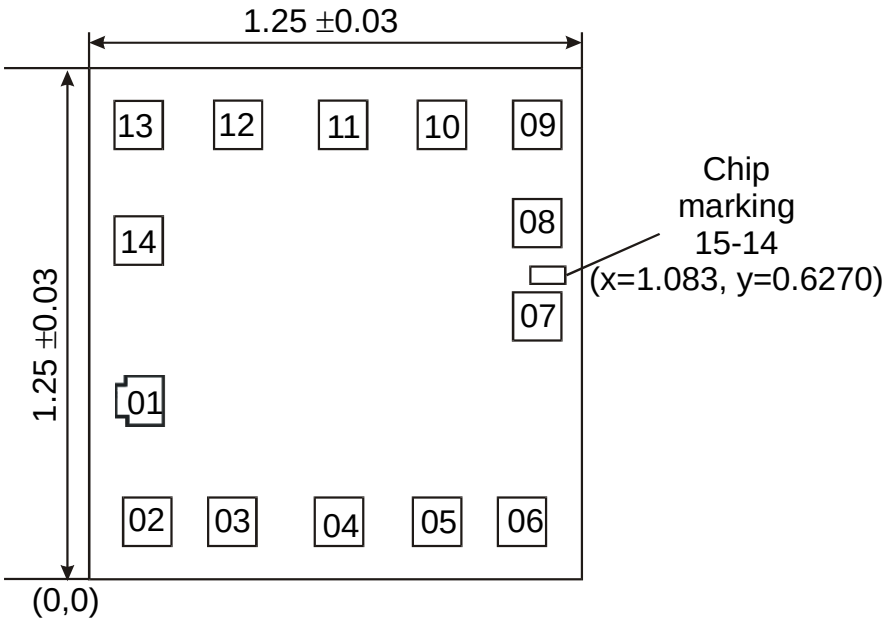


Figure 2. Test Circuit

CHIP PAD DIAGRAM IZ74HC14A



Pad size 0.106 x 0.106 mm (Pad size is given as per passivation layer)
Thickness of chip 0,46±0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	A1	0.14	0.345
02	Y1	0.14	0.141
03	A2	0.319	0.141
04	Y2	0.577	0.141
05	A3	0.817	0.141
06	Y3	1.019	0.141
07	GND	1.036	0.47
08	Y4	1.036	0.749
09	A4	1.006	1.007
10	Y5	0.8	1.007
11	A5	0.584	1.007
12	Y6	0.334	1.007
13	A6	0.141	0.969
14	V_{CC}	0.14	0.663