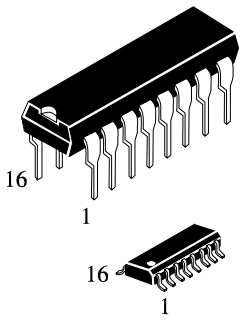
IN74HC174A

Hex D Flip-Flop with Common Clock and Reset

High-Performance Silicon-Gate CMOS



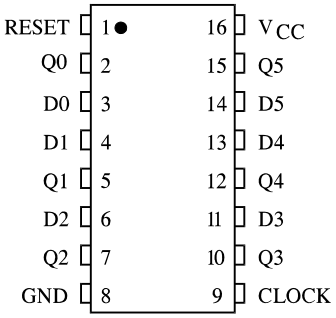
ORDERING INFORMATION
IN74HC174AN Plastic
IN74HC174AD SOIC
IZ74HC174A Chip
T_A = -55° to 125° C for all packages

The IN74HC174A is identical in pinout to the LS/ALS174. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

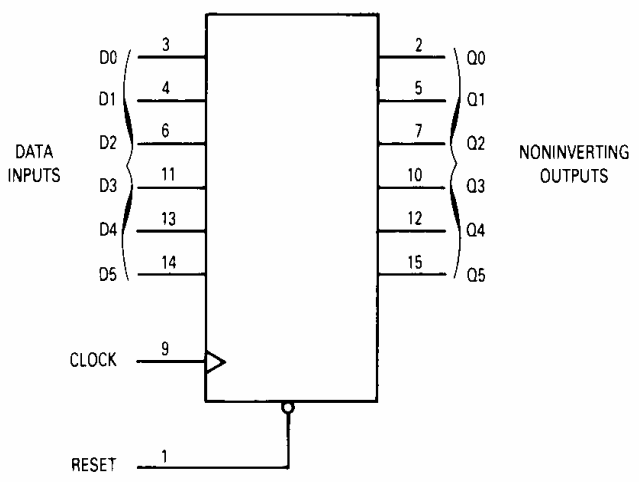
This device consists of six D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16=V_{CC}
PIN 8 = GND

FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	no change
H	↓	X	no change

X = Don't care

L = LOW voltage level

H = HIGH voltage level

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1,5 mm from Case for 4 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				-55°C to 25°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}≥ V_{CC}-0.1 V or ≤0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}≤0.1 V or ≥V_{CC}-0.1 V $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 4.0 mA $\|I_{OUT}\|$ ≤ 5.2 mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= V_{IL} or V_{IH} $\|I_{OUT}\|$ ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}= V_{IL} or V_{IH} $\|I_{OUT}\|$ ≤ 4.0 mA $\|I_{OUT}\|$ ≤ 5.2 mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6.0 ns, V_{IL}= 0 V, V_{IH}=Vcc)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			-55°C to 25°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 4.5 6.0	6.0 30 35	4.8 24 28	4.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0 4.5 6.0	110 22 19	140 28 24	165 33 28	ns
t_{PHL}	Maximum Propagation Delay , Reset to Q (Figures 2 and 4)	2.0 4.5 6.0	110 21 19	140 28 24	160 32 27	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 62	pF

TIMING REQUIREMENTS (C_L=50pF,Input t_r=t_f=6.0 ns, V_{IL}= 0 V, V_{IH}=Vcc)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			-55 °C to 25°C	≤85°C	≤125°C	
t_{SU}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t_w	Minimum Pulse Width, Reset (Figure 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

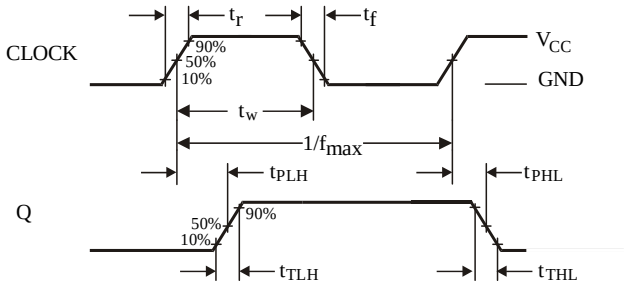


Figure 1. Switching Waveforms

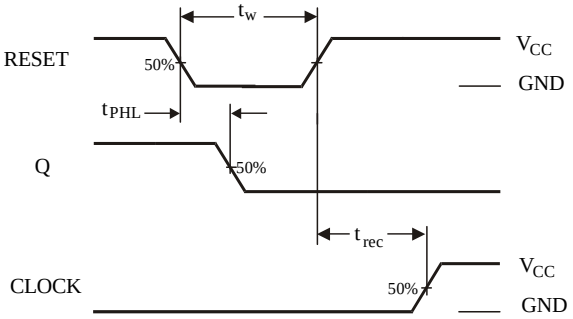


Figure 2. Switching Waveforms

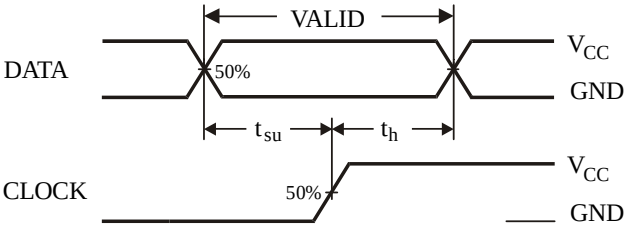


Figure 3. Switching Waveforms

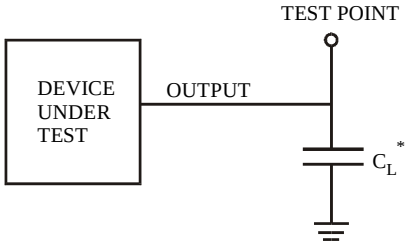
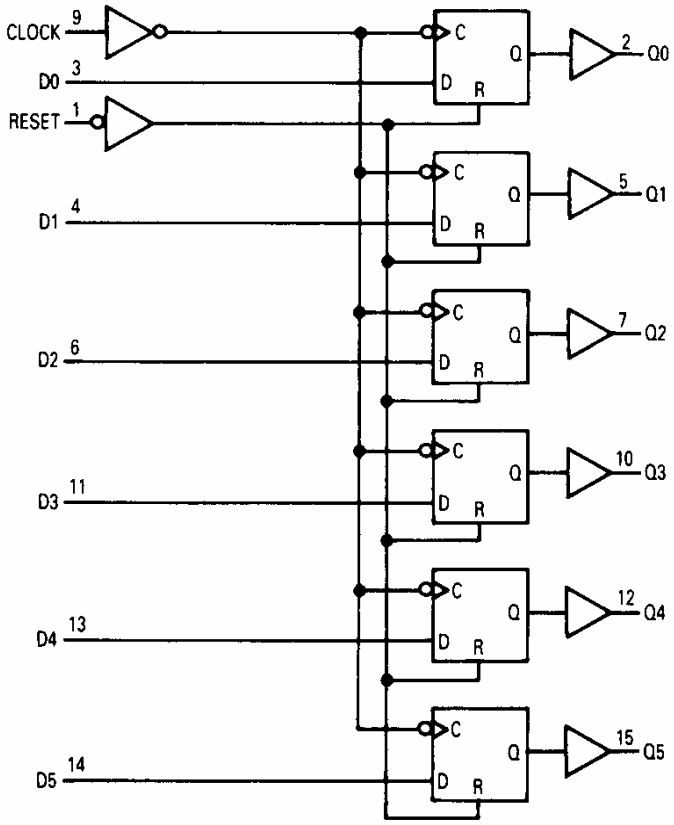
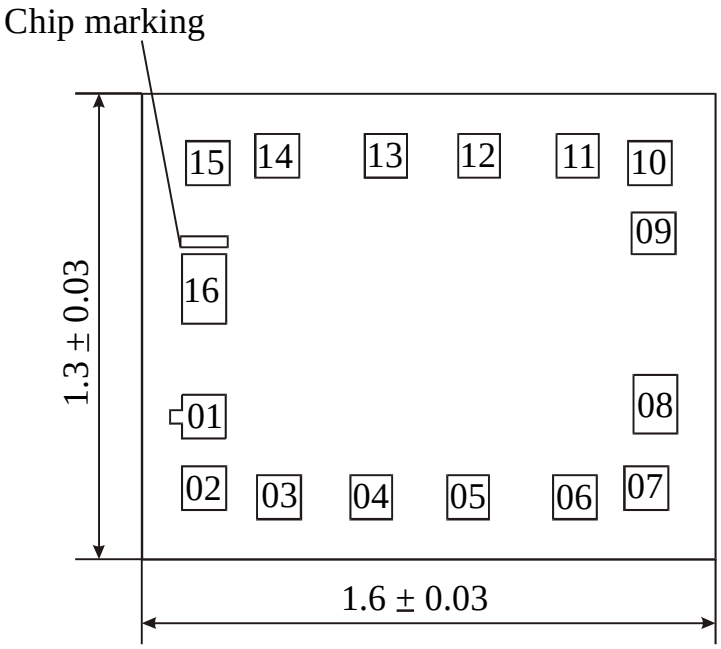


Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM



Chip marking :15HC174
Location of marking (mm): left lower corner x = 0.110, y = 0.870; right lower corner x = 0.240, y = 0.900
Chip thickness: 0.46 ± 0.02 mm

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	Reset	0.115	0.340	0.12×0.12
02	Q0	0.115	0.140	0.12×0.12
03	D0	0.325	0.115	0.12×0.12
04	D1	0.580	0.115	0.12×0.12
05	Q1	0.850	0.115	0.12×0.12
06	D2	1.145	0.115	0.12×0.12
07	Q2	1.345	0.140	0.12×0.12
08	GND	1.370	0.355	0.12×0.16
09	Clock	1.365	0.815	0.12×0.12
10	Q3	1.355	1.045	0.12×0.12
11	D3	1.155	1.065	0.12×0.12
12	Q4	0.880	1.065	0.12×0.12
13	D4	0.620	1.065	0.12×0.12
14	D5	0.320	1.065	0.12×0.12
15	Q5	0.125	1.045	0.12×0.12
16	Vcc	0.115	0.660	0.12×0.19

Note: Location is given as per passivation layer