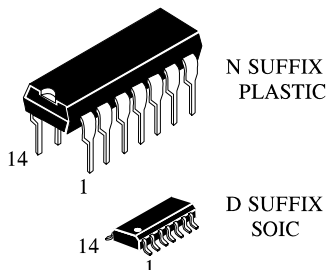


IN74HC00A

Quad 2-Input NAND Gate

The IN74HC00A is identical in pinout to the LS/ALS00. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices

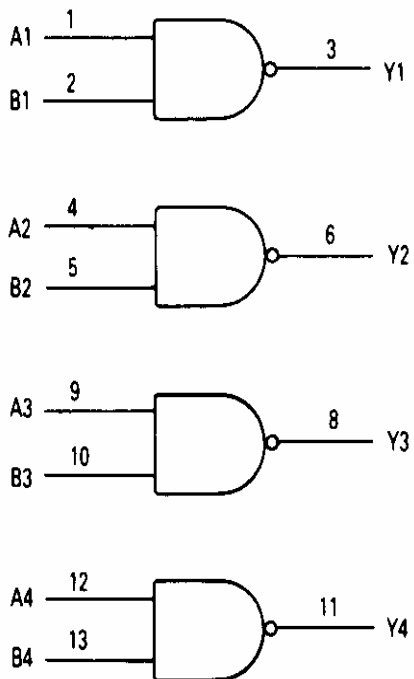


N SUFFIX PLASTIC

D SUFFIX SOIC

ORDERING INFORMATION
 IN74HC00AN Plastic
 IN74HC00AD SOIC
 IN72HC00A Chip
 $T_A = -55^\circ$ to 125° C for all packages

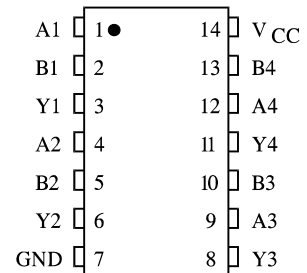
LOGIC DIAGRAM



$Y = \overline{AB}$

PIN 14 = V_{CC}
 PIN 7 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			ns
	V _{CC} =2.0 V	0	1000	
	V _{CC} =4.5 V	0	500	
	V _{CC} =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IL}	Maximum Low -Level Input Voltage	V _{OUT} =0.1 V or V _{CC} =0.1 V I _{OUT} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} =0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA	4.5	0.26	0.33	0.4	V
			6.0	0.26	0.33	0.4	
			V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 5.2 mA	2.0	1.9	1.9	
I _{IL}	Maximum Low-Level Input Leakage Current	V _{IL} =GND	4.5	3.98	3.84	3.7	μA
			6.0	5.48	5.34	5.2	
			V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 5.2 mA	6.0	-0.1	-1.0	
I _{IH}	Maximum High-Level Input Leakage Current	V _{IH} =V _{CC}	6.0	0.1	1.0	1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IL} =V _{CC} V _{IH} =GND I _{OUT} =0 μA	6.0	1.0	10	40	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	V _{IL} =0 V V _{IH} =V _{CC} t _{LH} =t _{HL} =6 ns C _L = 50 pF	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	V _{IL} =0 V V _{IH} =V _{CC} t _{LH} =t _{HL} =6 ns C _L = 50 pF	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C _{IN}	Maximum Input Capacitance		6.0	10	10	10	pF
C _{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: P _D =C _{PD} V _{CC} ² f+I _{CC} V _{CC}		5.0	T _A = 25°C, V _{CC} =5.0 V			pF

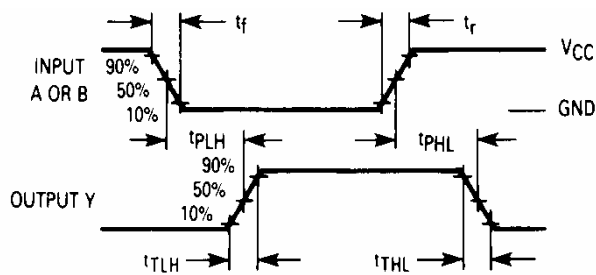
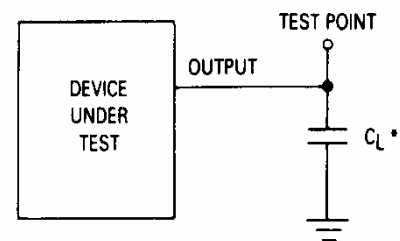


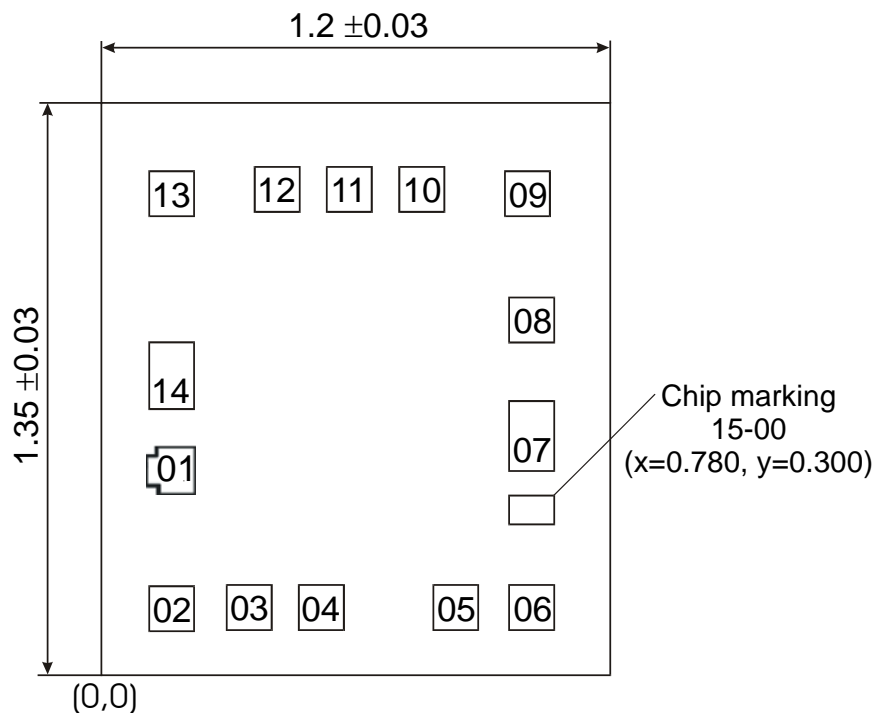
Figure 1. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 2. Test Circuit

PAD CHIP DIAGRAM IZ74HC00A



Pad size 0.108 x 0.108 mm (Pad size is given as per passivation layer)
Thickness of chip 0,46±0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	A1	0.132	0.443
02	D1	0.132	0.129
03	Y1	0.315	0.129
04	A2	0.485	0.129
05	B2	0.802	0.129
06	Y2	0.981	0.129
07	GND	0.981	0.504
08	Y3	0.981	0.807
09	A3	0.971	1.105
10	B3	0.722	1.115
11	Y4	0.551	1.15
12	A4	0.381	1.115
13	B4	0.132	1.105
14	Vcc	0.132	0.650