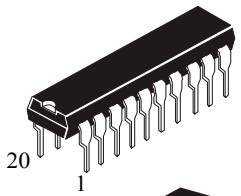
IN74LV245

OCTAL BUS TRANSCEIVER; 3-State

The IN74LV245 is a low-voltage Si-gate CMOS device and is pin and function compatible with IN74HCT245.

The IN74LV245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The IN74LV245 features an output enable ($\overline{OE}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{OE}$ controls the outputs so that the buses are effectively isolated.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL IC_S
- Supply voltage range: 1.2 to 3.6 V
- Low input current: 1.0 μA; 0.1 μA at T = 25 °C
- Output Current: 8 mA at V_{CC} = 3.0 V
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX
PLASTIC DIP

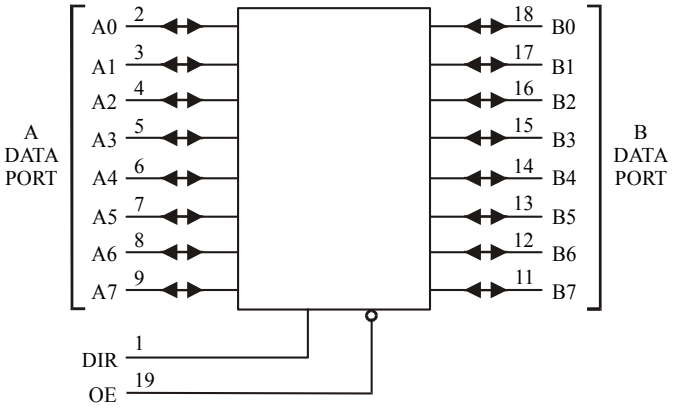
DW SUFFIX
SO

ORDERING INFORMATION

IN74LV245N	Plastic DIP
IN74LV245DW	SOIC
IZ74LV245	chip

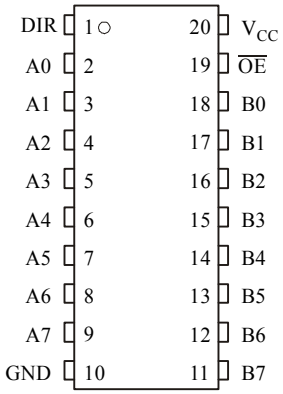
T_A = -40° to 125° C for all packages

LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Inputs/outputs	
$\overline{OE}$	**DIR**	**A**	**B**
L	L	A=B	input
L	H	input	B=A
H	X	Z	Z

H= high level
L = low level
X = don't care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +5.0	V
I_{IK} *1	DC Input diode current	±20	mA
I_{OK} *2	DC Output diode current	±50	mA
I_O *3	DC Output source or sink current	±35	mA
I_{CC}	DC V_{CC} current	±70	mA
I_{GND}	DC GND current	±70	mA
P_D	Power dissipation per package: *4 Plastic DIP SO	 750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*1 $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V.
*2 $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V.
*3 -0.5 V $< V_O < V_{CC} + 0.5$ V.
*4 Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SO Package: : - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.2	3.6	V
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =1.2 V V_{CC} =2.0 V V_{CC} =3.0 V V_{CC} =3.6 V	0 0 0 0	1000 700 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
V_{IH}	HIGH level input voltage		1.2 2.0 3.0 3.6	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	V
V_{IL}	LOW level input voltage		1.2 2.0 3.0 3.6	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	V
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = -50 μA	1.2 2.0 3.0 3.6	1.1 1.92 2.92 3.52	- - - -	1.0 1.9 2.9 3.5	- - - -	1.0 1.9 2.9 3.5	- - - -	V
		$V_I = V_{IH}$ or V_{IL} I_O = -8 mA	3.0	2.48	-	2.34	-	2.20	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = 50 μA	1.2 2.0 3.0 3.6	- - - -	0.09 0.09 0.09 0.09	- - - -	0.1 0.1 0.1 0.09	- - - -	0.1 0.1 0.1 0.09	V
		$V_I = V_{IH}$ or V_{IL} I_O = 8 mA	3.0	-	0.33	-	0.4	-	0.5	V
I_I	Input current	$V_I = V_{CC}$ or 0 V	*	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	Three state leakage current	3-state outputs V_I (19) = V_{IH} $V_O = V_{CC}$ or 0 V	1.2 *	-	±0.5	-	±5	-	±10	μA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0 V I_O = 0 μA	*	-	8.0	-	80	-	160	μA

* V_{CC} = 3.3 ± 0.3 V

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, t_r=t_f=6.0 ns, R_L = 1 kΩ)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH}	Propagation delay , An to Bn, Bn to An	V_I = 0 V or V_{CC} Figure 1	1.2	-	100	-	125	-	140	ns
			2.0	-	23	-	28	-	34	
			*	-	14	-	18	-	21	
t_{PHZ}, t_{PLZ}	Propagation delay, OE, DIR to An, Bn	V_I = 0 V or V_{CC} Figure 2	1.2	-	120	-	140	-	160	ns
			2.0	-	30	-	37	-	43	
			*	-	20	-	24	-	28	
t_{PZH}, t_{PZL}	Propagation delay, OE to An, Bn	V_I = 0 V or V_{CC} Figure 2	1.2	-	120	-	140	-	160	ns
			2.0	-	28	-	35	-	43	
			*	-	17	-	21	-	26	
t_{THL}, t_{TLH}	Output Transition Time, Any Output	V_I = 0 V or V_{CC} Figure 1	1.2	-	60	-	75	-	90	ns
			2.0	-	16	-	20	-	24	
			*	-	10	-	13	-	15	
C_I	Input capacitance	For inputs 01,19	3.0	-	7.0	-	-	-	-	pF
$C_{I/O}$	Input/output capacitance	For inputs/ outputs 02-09, 11-18	3.0	-	20	-	-	-	-	pF
C_{PD}	Power dissipation capacitance (per one channel)	V_I = 0 V or V_{CC}		-	50	-	-	-	-	pF

* V_{CC} = 3.3 ± 0.3 V

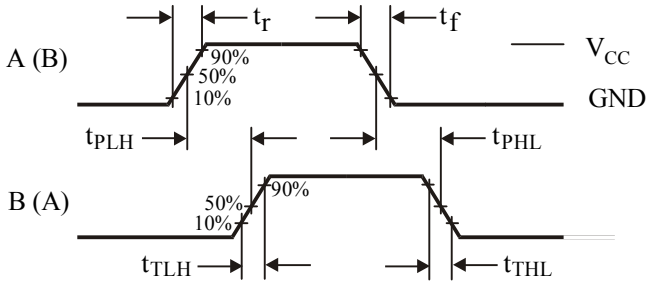


Figure 1. Switching Waveforms

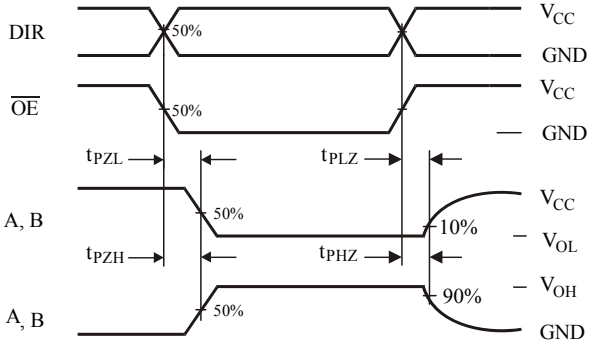
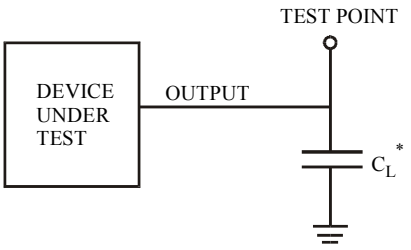
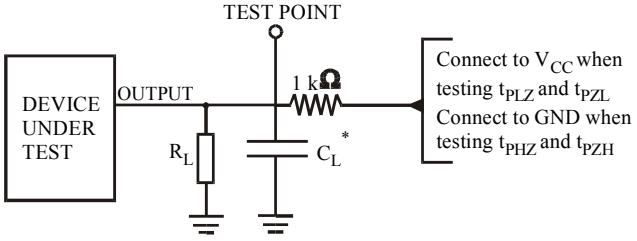


Figure 2. Switching Waveforms



* Includes all probe and jig capacitance

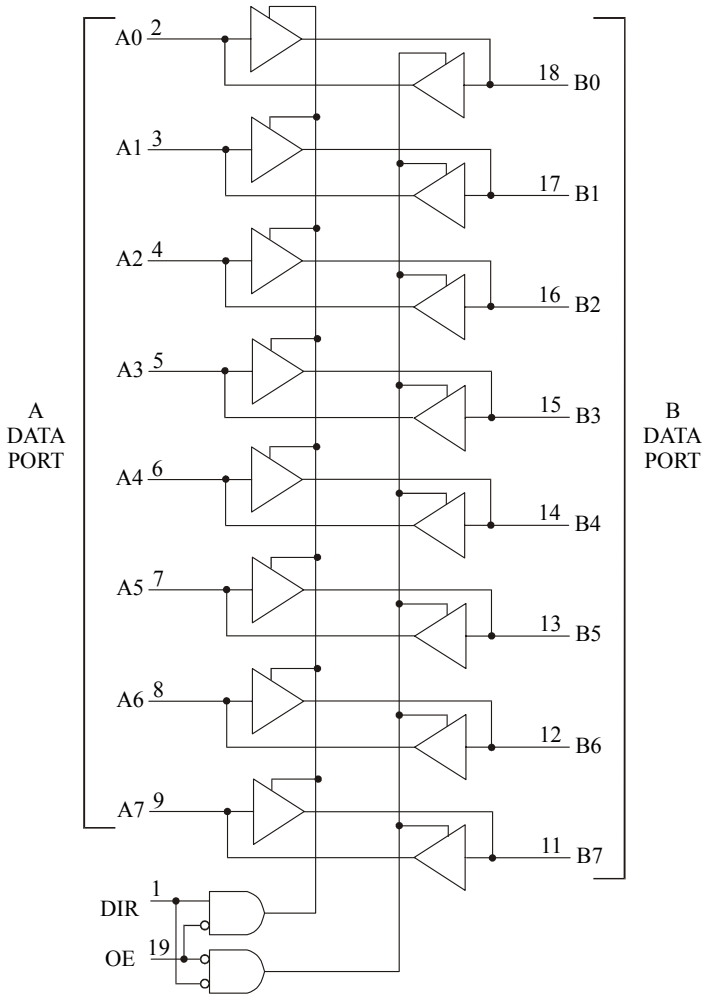
Figure 3. Test Circuit



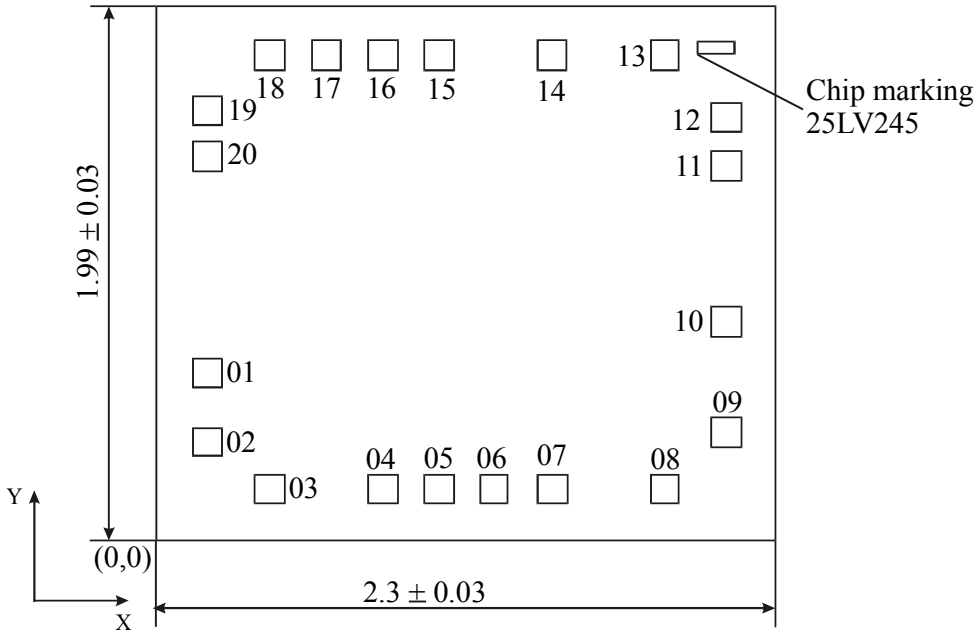
* Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x=2.010, y=1.810.

Chip thickness: 0.46 ± 0.02 mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	DIR	0.140	0.573	0.108 x 0.108
02	A0	0.140	0.315	0.108 x 0.108
03	A1	0.370	0.140	0.108 x 0.108
04	A2	0.790	0.140	0.108 x 0.108
05	A3	1.000	0.140	0.108 x 0.108
06	A4	1.200	0.140	0.108 x 0.108
07	A5	1.417	0.140	0.108 x 0.108
08	A6	1.833	0.140	0.108 x 0.108
09	A7	2.060	0.354	0.108 x 0.108
10	GND	2.060	0.760	0.108 x 0.108
11	B7	2.060	1.340	0.108 x 0.108
12	B6	2.060	1.520	0.108 x 0.108
13	B5	1.833	1.750	0.108 x 0.108
14	B4	1.415	1.750	0.108 x 0.108
15	B3	1.000	1.750	0.108 x 0.108
16	B2	0.790	1.750	0.108 x 0.108
17	B1	0.580	1.750	0.108 x 0.108
18	B0	0.370	1.750	0.108 x 0.108
19	$\overline{OE}$	0.140	1.544	0.108 x 0.108
20	V_{CC}	0.140	1.375	0.108 x 0.108

Note: Pad location is given as per metallization layer