# *CLASS D AUDIO AMPLIFIER*

**(compatible to ILA8933)**

The ILA8933 is a high efficiency class-D amplifier with low power dissipation.
The continuous time output power is 2 x 10 W in a stereo half bridge application ($R_L$ = 8Ω) or 1 x 20 Win a mono full bridge application ($R_L$ =16 W). Due to the low power dissipation the device can be used without any external heat sink, even for application with high supply voltages and/or lower load impedances.
The device has two full differential inputs driving two independent outputs. It can be used in a mono full bridge configuration (Bridge-Tied Load (BTL)) or a stereo half bridge configuration (Single-Ended (SE)).
The ILA8933 is designed for TV sets, monitors Multimedia systems, home sound sets

## Main features

- High efficiency
- Application without heat sink
- Operating voltage
  - 10 V to 36 V asymmetrical
  - ± 5 V to ± 18 V symmetrical
- Thermal protection
- Current limiting to avoid audio holes
- Short circuit protection
- Switchable internal / external oscillator (master-slave setting)
- No pop noise
- Low power dissipation
- Mono bridge-tied load (full bridge) or stereo single-ended (half bridge) application Full differential inputs

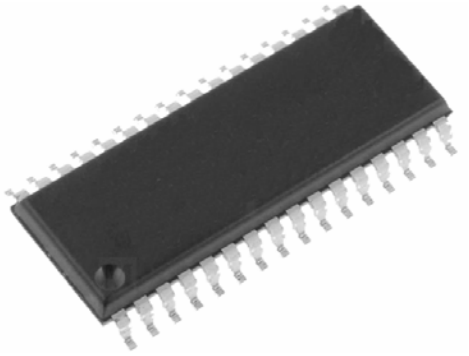


**Fig. 1. General view**

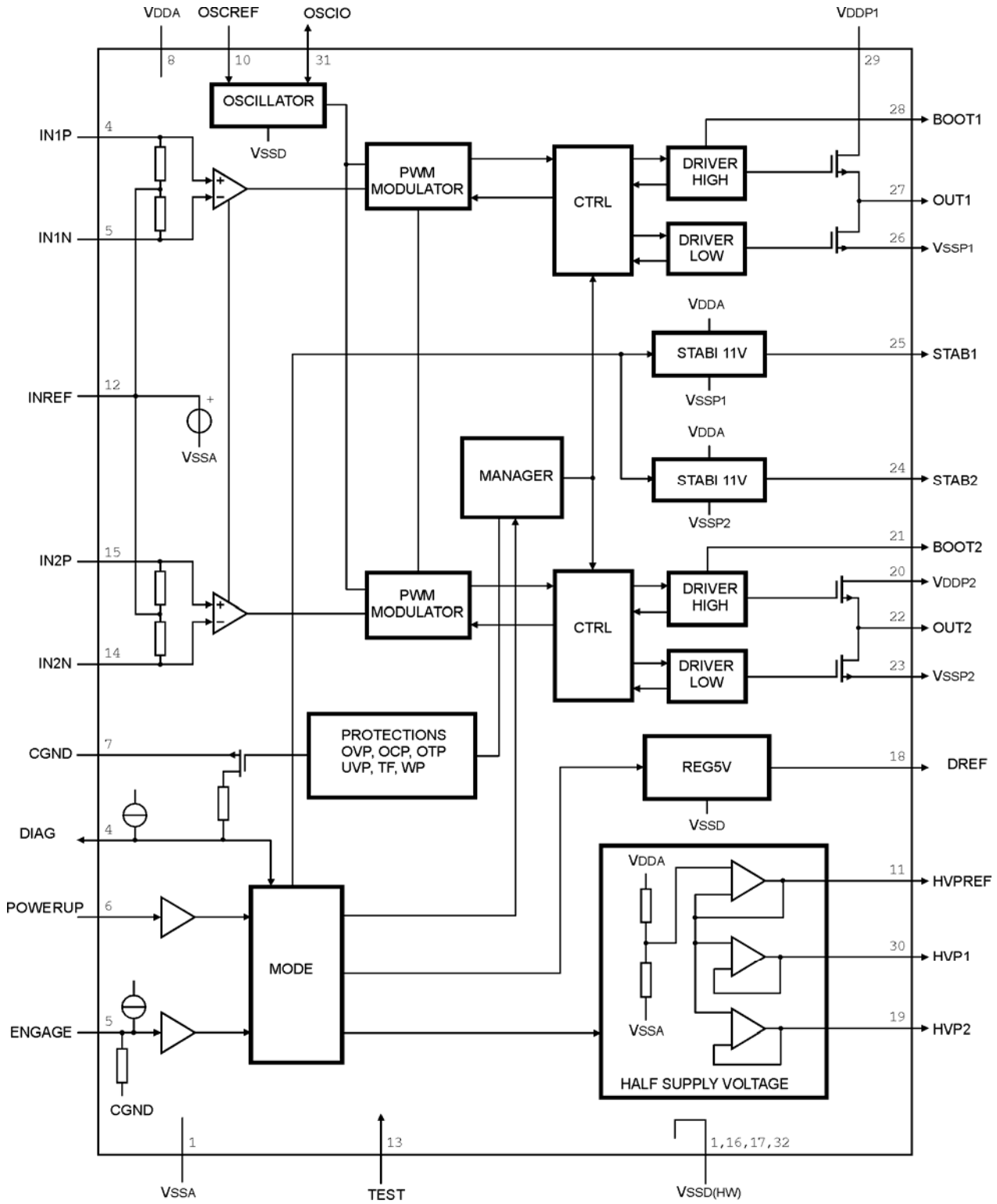



**Fig. 2. Block Diagram**

**Table 1 –Pin Description**

| Symbol | Pin | Description |
|---|---|---|
| $V_{SSD(HW)}$ | 1 | Negative digital supply voltage and handle wafer connection |
| IN1P | 2 | Positive audio input for channel 1 |
| IN1N | 3 | Negative audio input for channel 1 |
| DIAG | 4 | Diagnostic output; open-drain |
| ENGAGE | 5 | Engage input to switch between Mute mode and Operating mode |
| POWERUP | 6 | Power-up input to switch between Sleep mode and Mute mode |
| $C_{GND}$ | 7 | Control ground; reference for POWERUP, ENGAGE and DIAG |
| $V_{DDA}$ | 8 | Positive analog supply voltage |
| $V_{SSA}$ | 9 | Negative analog supply voltage |
| OSCREF | 10 | Input internal oscillator setting (only master setting) |
| HVPREF | 11 | Decoupling of internal half supply voltage reference |
| INREF | 12 | Decoupling for input reference voltage |
| TEST | 13 | Dest signal input; for testing purpose only |
| IN2N | 14 | Negative audio input for channel 2 |
| IN2P | 15 | Positive audio input for channel 2 |
| $V_{SSD(HW)}$ | 16 | Negative digital supply voltage and handle wafer connection |
| $V_{SSD(HW)}$ | 17 | Negative digital supply voltage and handle wafer connection |
| DREF | 18 | Decoupling of internal (reference) 5 V regulator for logic supply |
| HVP2 | 19 | Half supply output voltage 2 for charging single-ended capacitor for channel 2 |
| $V_{DDP2}$ | 20 | Positive power supply voltage for channel 2 |
| BOOT2 | 21 | Bootstrap high-side driver channel 2 |
| OUT2 | 22 | Pulse Width Modulated (PWM) output channel 2 |
| $V_{SSP2}$ | 23 | Negative power supply voltage for channel 2 |
| STAB2 | 24 | Decoupling of internal 11 V regulator for channel 2 drivers |
| STAB1 | 25 | Decoupling of internal 11 V regulator for channel 1 drivers |
| $V_{SSP1}$ | 26 | Negative power supply voltage for channel 1 |
| OUT1 | 27 | PWM output channel 1 |
| BOOT1 | 28 | Bootstrap capacitor for channel 1 |
| $V_{DDP1}$ | 29 | Positive power supply voltage for channel 1 |
| HVP1 | 30 | Half supply output voltage 1 for charging single-ended capacitor for channel 1 |
| OSCIO | 31 | Oscillator input in slave configuration or oscillator output in master configuration |
| $V_{SSD(HW)}$ | 32 | Negative digital supply voltage and handle wafer connection |

**Table 2 – Maximum rating & recommended operating conditions**

| Parameter, unit | | Symbol | Recommended operating conditions | | Maximum rating | |
|---|---|---|---|---|---|---|
| | | | Target | | Target | |
| | | | Min | Max | Min | Max |
| Ambient temperature, °C | | Ta | -40 | 85 | -55 | +150 |
| Dissipated power[1], W | | P | – | – | – | $\frac{150^0\,C - T_a}{R_{TjA}}$ |
| Supply voltage for asymmetrical supply, V | | $U_P$ | 10 | 36 | -0,3 | +40 |
| Voltage on pins, V | IN1P, IN1N, IN2P, IN2N [2] | Ux | – | – | -5 | 5 |
| | OSCREF, OSCIO [3] | | – | – | $U_{SSD(HW)}$ - 0.3 | 5 |
| | POWERUP, ENGAGE, DIAG [4] | | – | – | $U_{CGND}$ - 0.3 | 6 |
| | Rest of pins [5] | | – | – | $U_{SS}$ - 0.3 | $U_{DD}$ + 0.3 |
| Repetitive output peak current, A | | $I_{ORM}$ [6] | – | – | 2,3 | – |

[1] Typical value $R_{TjA}$ = 44°C/W

[2] Measured with respect to pin INREF; $U_X < U_{DD}$ + 0,3 B.

[3] Measured with respect to pin $U_{SSD(HW)}$; $U_X < U_{DD}$ + 0,3 B.

[4] Measured with respect to pin CGND; $U_X < U_{DD}$ + 0,3 B.

[5] $U_{SS} = U_{SSP1} = U_{SSP2}$; $U_{DD} = U_{DDP1} = U_{DDP2}$.

[6] Current limiting concept.

**Table 3 – Electric parameters**

(Up = 25 V, Fosc = 320 kHz, Ta = 25°C, unless otherwise specified.)

| Parameter, unit | Symbol | Measurement mode | Target | |
|---|---|---|---|---|
| | | | Min | Max |
| 1 | 2 | 3 | 4 | 5 |
| Supply voltage, V | $U_P$ | Asymmetrical supply | 10 | 36 |
| | | Symmetrical supply | ±5 | ±18 |
| Supply current, mA | $I_P$ | Sleep mode | – | 1,0 |
| Total quiescent current, mA | Iq(tot) | No load | – | 50 |
| Pin POWERUP[1)] input voltage, V | $U_{I6}$ | – | 0 | 6,0 |
| Pin POWERUP input current, μA | $I_{I6}$ | $U_{I6}$ = 3 V | – | 20 |
| Pin POWERUP[1)] low level input voltage, V | $U_{IL6}$ | – | 0 | 0,8 |
| Pin POWERUP [1)] high level input voltage, V | $U_{IH6}$ | – | 2 | 6 |
| Pin ENGAGE[1)] output voltage, V | $U_{O5}$ | – | 4,2 | 5,0 |
| Pin ENGAGE[1)] input voltage, V | $U_{I5}$ | – | 0 | 6,0 |
| Pin ENGAGE output current, μA | $I_{O5}$ | $U_{I5}$ = 3 V | – | 40 |
| Pin ENGAGE[1)] low level input voltage, V | $U_{IL5}$ | – | 0 | 0,8 |
| Pin ENGAGE [1)] high level input voltage, V | $U_{IH5}$ | – | 3 | 6 |
| Pin DIAG [1)] output voltage,V | $U_{O4}$ | Protection activated | – | 0,8 |
| | | Operating mode | 2 | 3,3 |
| Pins HVP1, HVP2 output voltage, V | $U_{O30}$, $U_{O19}$ | – | $0,5U_P$-0,2 | $0,5U_P$+0,2 |
| HVPREF pin output voltage, V | $U_{O11}$ | – | $0,5U_P$-0,2 | $0,5U_P$+0,2 |

**Table 3 (continued)**

| 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|
| Reference voltage for digital part, V | $U_{O18}$ | – | 4,5 | 5,1 |
| Output offset voltage OUT1, OUT2, mV | $U_{offset}$ | Two channel mode with respect to HVPREF | | |
| | | Mute mode | – | 15 |
| | | Operating mode | – | 100 |
| | | BTL | | |
| | | Mute mode | – | 20 |
| | | Operating mode | – | 150 |
| Pins STAB1, STAB2 stabilized output voltage, V | $U_{STAB24}$, $U_{STAB25}$ | Mute mode, operating mode with respect to $U_{SSP1}$, $U_{SSP2}$ | 10 | 12 |
| Undervoltage protection threshold supply voltage, V | $U_{P(uvp)}$ | – | 8,0 | 9,9 |
| Overvoltage protection threshold supply voltage, V | $U_{P(ovp)}$ | – | 36,1 | 40 |
| Low unbalance protection threshold supply voltage, V | $U_{P(th)(ubp)l}$ | $U_{HVPREF}$ = 11B | – | 18 |
| High unbalance protection threshold supply voltage, V | $U_{P(th)(ubp)h}$ | $U_{HVPREF}$ = 11B | 29 | – |
| Overcurrent protection output current, A | $I_{O(ocp)}$ | – | 2,0 | – |
| Thermal protection activation temperature, °C | $T_{act(th\_prot)}$ | – | 155 | 160 |
| Thermal foldback activation temperature, °C | $T_{act(th\_fold)}$ | – | 140 | 150 |
| Pin OSCIO [2] high level input voltage, V | $U_{IH31}$ | – | 4,0 | 5,0 |
| Pin OSCIO [2], low level input voltage, V | $U_{IL31}$ | – | 0 | 0,8 |
| Pin OSCIO [2] high level output voltage, V | $U_{OH31}$ | – | 4,0 | 5,0 |
| Pin OSCIO [2], low level output voltage, V | $U_{OL31}$ | – | 0 | 0,8 |
| Maximum number of slaves driven by one master | $N_{slave(max)}$ | – | 12 | – |
| Internal oscillator frequency, kHz | $F_{OSC}$ | – | 300 | 500 |
| **SE mode (Up = 25 V, $R_L$= 2x8 Ω, $F_{OSC}$ = 320 kHz, $f_i$ = 1 kHz, $R_S$ < 0,1 Ω [3], Ta = 25°C)** | | | | |
| RMS output power, W | $P_{O(RMS)}$ | $R_L$ = 4 Ω, Up = 17 V [4] | | |
| | | THD+N = 0,5%, $f_i$ = 1 kHz | 5,9 | – |
| | | THD+N = 10%, $f_i$ = 1 kHz | 7,5 | – |
| | | $R_L$ = 8 Ω, Up = 25 V | | |
| | | THD+N = 0,5%, $f_i$ = 1 kHz | 7,3 | – |
| | | THD+N = 10%, $f_i$ = 1 kHz | 9,3 | – |
| | | $R_L$ = 8 Ω, Up = 31 V | | |
| | | THD+N = 0,5% | 11,2 | – |
| | | THD+N = 10% | 14,1 | – |

**Table 3 (continued)**

| 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|
| Total harmonic distortion-plus-noise, % | THD+N | $P_O$ = 1 W | | |
| | | $f_i$ = 1 kHz | – | 0,1 |
| | | $f_i$ = 6 kHz | – | 0,1 |
| Closed-loop voltage gain, dB | $G_{U(CL)}$ | $U_I$ = 100 mV, no load | 29 | 31 |
| Voltage gain difference, dB | $\Delta\|G_U\|$ | – | | 1 |
| Channel separation, dB | $\alpha_{CS}$ | $P_O$ = 1 W, $f_i$ = 1 kHz | 70 | – |
| Supply voltage ripple rejection, dB | SVRR | Operating mode | | |
| | | $f_i$ = 1 kHz | 40 | – |
| Input impedance, kΩ | $\|Z_I\|$ | | 70 | – |
| Noise level, μV | $U_{n(o)}$ | Operating mode, $R_S$ = 0 Ω | – | 150 |
| | | Mute mode | – | 100 |
| Efficiency, % | $\eta_{po}$ | $P_O$ = 10 W | | |
| | | Up = 17V, $R_L$ = 4 Ω | 86 | – |
| | | Up = 25 V, $R_L$ = 8 Ω | 89 | – |
| **BTL mode ( Up = 25 V, $R_L$= 16Ω, $F_{OSC}$ = 320 kHz, $f_i$ = 1 kHz, $R_S$ < 0,1 Ω [3], Ta = 25°C)** | | | | |
| RMS output power, W | $P_{O(RMS)}$ | $R_L$ = 8 Ω, Up = 17 V [4] | | |
| | | THD+N = 0,5%, $f_i$ = 1 kHz | 11,9 | – |
| | | THD+N = 10%, $f_i$ = 1 kHz | 15,4 | – |
| | | $R_L$ = 16 Ω, Up = 25 V | | |
| | | THD+N = 0,5%, $f_i$ = 1 kHz | 14,9 | – |
| | | THD+N = 10%, $f_i$ = 1 kHz | 18,9 | – |
| | | $R_L$ = 16 Ω, Up = 31 V | | |
| | | THD+N = 0,5% | 22,8 | – |
| | | THD+N = 10% | 28,8 | – |
| Total harmonic distortion-plus-noise, % | THD+N | $P_O$ = 1 W | – | – |
| | | $f_i$ = 1 kHz | – | 0,1 |
| | | $f_i$ = 10 kHz | – | 0,24 |
| Closed-loop voltage gain, dB | $G_{V(CL)}$ | – | 35 | 37 |
| Input impedance, kΩ | $\|Z_I\|$ | – | 35 | – |
| Noise level, μV | $U_{n(o)}$ | $R_S$ = 0 Ω | | |
| | | Operating mode | – | 150 |
| | | Mute mode | – | 100 |
| Efficiency, % | $\eta_{po}$ | $P_O$ = 17 W, Up = 17 V, $R_L$ = 8 Ω | 87 | – |
| | | $P_O$ = 17 W, Up = 25 V, $R_L$ = 16 Ω | 90 | – |

[1] Measured with respect to pin CGND.
[2] Measured with respect to pin $V_{SSD(HW)}$.
[3] $R_S$ is the series resistance of inductor and capacitor of low-pass LC filter in the application.
[4] Output power is measured indirectly; based on RDSon measurement.

**Table 4 – Typical parameters ($U_P$ = 25V, Ta = 25°C)**

| Parameter, unit | Symbol | Measurement mode | Typical value[1)] |
|---|---|---|---|
| Drain-source on-state resistance, mΩ | $R_{DSon}$ | $T_j$ = 25°C | 350 |
| | | $T_j$ = 125°C | 545 |
| Bias output voltage, V | $U_{O(bias)}$ | With respect to $U_{SSA}$ | 2,1 |
| HVP1, HVP2 pins output current, mA | $I_{O19}$, $I_{O30}$ | $U_{HVP1} = U_{HVP2} = U_O - 1$ V | 50 |
| Internal oscillator frequency, kHz | $F_{OSC}$ | $R_{OSC}$ = 39 kΩ | 320 |
| Output signal rise time, ns | $t_r$ | Io = 0 A | 10 |
| Output signal fall time, ns | $t_f$ | Io = 0 A | 10 |
| Minimum output pulse width, ns | $t_{w(min)}$ | Io = 0 A | 80 |
| **SE mode(Up = 25 V, $R_L$= 2x8 Ω, $F_{OSC}$ = 320 kHz, $f_i$ = 1 kHz, $R_S$ < 0,1 Ω [2)], Ta = 25°C)** | | | |
| RMS output power, W | $P_{O(RMS)}$ | **$R_L$ = 4 Ом, Up = 17 В [3)]** | |
| | | THD+N = 0,5%, $f_i$ = 100 Hz | 6,5 |
| | | THD+N = 10%, $f_i$ = 100 Hz | 8,3 |
| | | **$R_L$ = 8 Ω, Up = 25 V** | |
| | | THD+N = 0,5%, $f_i$ = 100 Hz | 8,1 |
| | | THD+N = 10%, $f_i$ = 100 Hz | 10,3 |
| Supply voltage rejection ratio, dB | SVRR | Operating mode $f_i$ = 100 Hz | 60 |
| Output voltage, μV | $U_{O(mute)}$ | Mute mode, $U_I$ = 1 V (RMS) | 100 |
| Common mode rejection ratio , dB | CMRR | $U_{I(cm)}$ = 1 V (RMS) | 75 |
| **BTL mode (Up = 25 V, $R_L$= 16Ω, $F_{OSC}$=320 kHz, $f_i$ = 1 kHz, $R_S$ < 0,1 Ω [2)], Ta = 25°C)** | | | |
| RMS output power, W | $P_{O(RMS)}$ | **$R_L$ = 8 Ω, Up = 17 V [3)]** | |
| | | THD+N = 0,5%, $f_i$ = 100 Hz | 13,2 |
| | | THD+N = 10%, $f_i$ = 100 Hz | 17,1 |
| | | **$R_L$=16 Ω, Up = 25 V** | |
| | | THD+N = 0,5%, $f_i$ = 100 Hz | 16,5 |
| | | THD+N = 10%, $f_i$ = 100 Hz | 21 |
| Output voltage, μV | $U_{O(mute)}$ | Mute mode, $U_I$ = 1 V (RMS) | 100 |
| Common mode rejection ratio , dB | CMRR | $U_{I(cm)}$ = 1 V (RMS) | 75 |

[1)] $R_S$ is the series resistance of inductor and capacitor of low-pass LC filter in the application.
[2)] Output power is measured indirectly; based on RDSon measurement.

## FUNCTIONAL DESCRIPTION

The ILA8933 is a mono full bridge or stereo half bridge audio power amplifier using class-D technology. The audio input signal is converted into a Pulse Width Modulated (PWM) signal via an analog input stage and PWM modulator. To enable the output power DMOS transistors to be driven, this digital PWM signal is applied to control and handshake block and driver circuits for both the high side and low side. A 2nd-order-low-pass filter converts the PWM signal to an analog audio signal across the loudspeakers.

The ILA8933 contains two independent half bridges with full differential input stages. The loudspeakers can be connected in the following configurations:

- Mono full bridge: Bridge Tied Load (BTL)
- Stereo half bridge: Single-Ended (SE)

The ILA8933 contains circuits common to both channels, such as: the oscillator, all reference sources, the mode functionality and a digital timing manager.

The following protections are built-in: thermal foldback, temperature, current and voltage.

### Operation modes

The ILA8933 can be switched to one of four operating modes using pins POWERUP and ENGAGE:

- Sleep mode: with low supply current;
- Mute mode: the amplifiers are switching idle (50 % duty cycle), but the audio signal at the output is suppressed by disabling the VI-converter input stages. The capacitors on pins HVP1 and HVP2 have been charged to half the supply voltage (asymmetrical supply only);
- Operating mode: the amplifiers are fully operational with an output signal;
- Fault mode;

Both pins POWERUP and ENGAGE refer to pin CGND.

**Table 4. Mode selection**

| Mode | Pin | | |
|---|---|---|---|
| | POWERUP[1)] | ENGAGE[1)] | DIAG |
| Sleep | < 0.8 V | < 0.8 V | undefined |
| Mute | 2 V to 6 V | < 0.8 V | > 2 V |
| Operating | 2 V to 6 V | 3 V to 6 V | > 2 V |
| Fault | 2 V to 6 V | undefined | < 0.8 V |

[1] When there are symmetrical supply conditions, the voltage applied to pins POWERUP and ENGAGE must never exceed the supply voltage ($V_{DDA}$, $V_{DDP1}$ or $V_{DDP2}$).

**PWM frequency**

The output signal of the amplifier is a PWM signal with a carrier frequency of approximately 320 kHz. Using a 2nd-order-low-pass filter in the application results in an analog audio signal across the loudspeaker. The PWM switching frequency can be set by an external resistor Rosc connected between pin OSCREF and $V_{SSD(HW)}$. The carrier frequency can be set between 300 kHz and 500 kHz. Using an external resistor of 39 kΩ, the carrier frequency is set to an optimized value of 320 kHz.

If two or more ILA8933 devices are used in the same audio application, it is recommended to synchronize the switching frequency of all devices. This can be done by connecting all the OSCIO pins together and configuring one of the ILA8933 devices in the application as the clock master. Configure the other ILA8933 devices as slaves.

Pin OSCIO is a 3-state input or output buffer. Pin OSCIO is configured in master mode as oscillator output, and in slave mode as oscillator input. Master mode is enabled by applying a resistor between pin OSCREF and VSSD(HW), while slave mode is enabled by connecting pin OSCREF directly to $V_{SSD(HW)}$ (without any resistor).

The value of the resistor also sets the frequency of the carrier and can be calculated with

$$f_{OSC} = \frac{12.45 \times 10^9}{R_{OSC}};$$

Where:

fosc = oscillator frequency (Hz)

Rosc = oscillator resistor (Ω) (on pin OSCREF)

**Table 5. Master/slave configuration**

| Configuration | Pin | |
|---|---|---|
| | **OSCREF** | **OSCIO** |
| Master | $R_{osc}$ > 25 kW to $V_{SSD(HW)}$ | output |
| Slave | $R_{osc}$ = 0 W; shorted to $V_{SSD(HW)}$ | input |

**Protections**

The following protections are implemented in the ILA8933:

- Thermal Foldback (TF);
- OverTemperature Protection (OTP);
- OverCurrent Protection (OCP);
- Window Protection (WP);
- Supply voltage protections;
  - UnderVoltage Protection (UVP);
  - OverVoltage Protection (OVP);
  - UnBalance Protection (UBP);
- ElectroStatic Discharge (ESD)

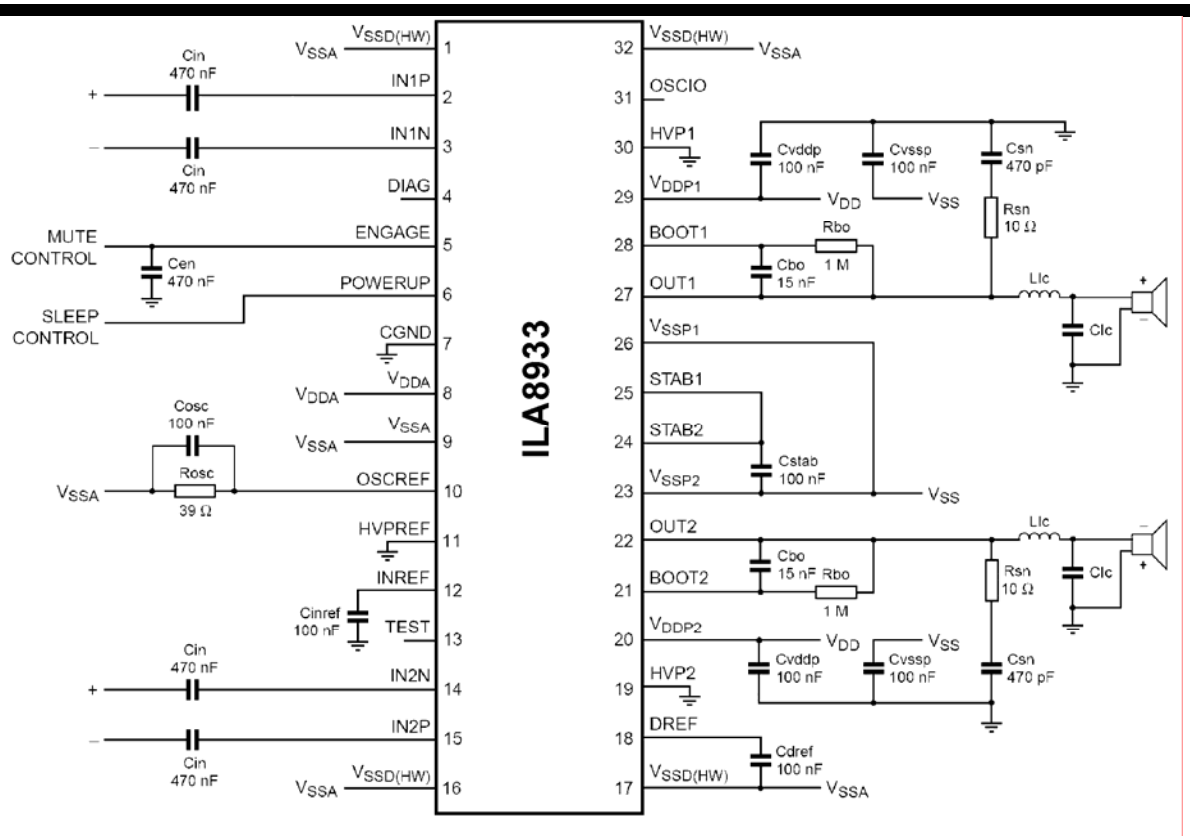



**Fig.3 Application diagram for 2 × SE (symmetrical supply)**

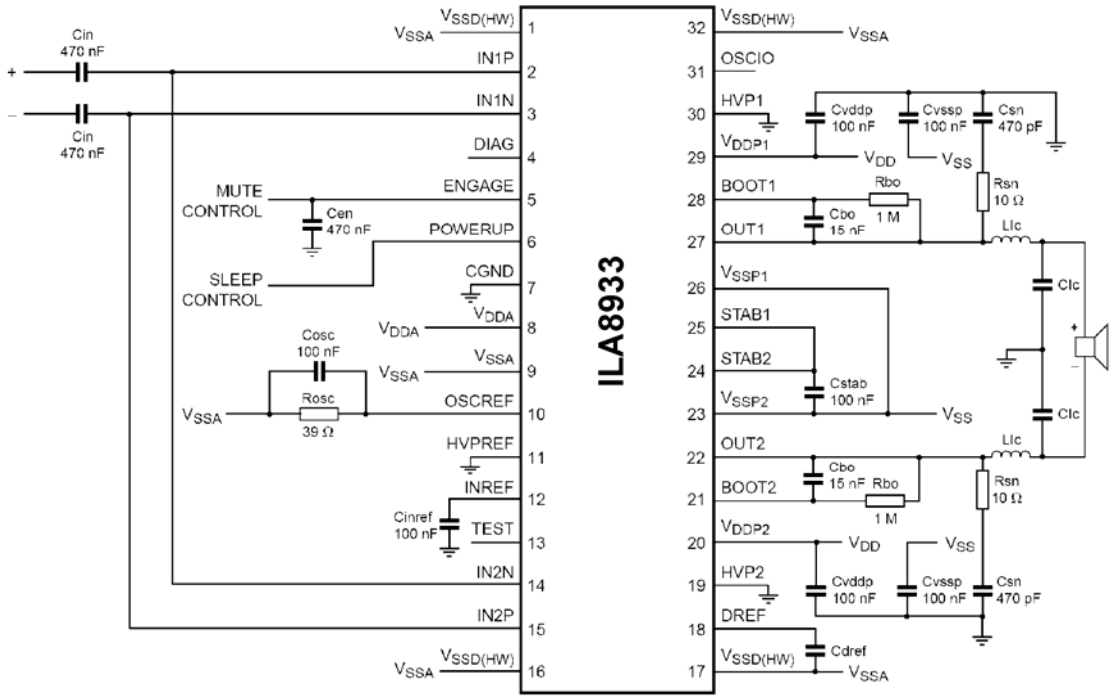



**Fig.4 Application diagram for 1 × BTL (symmetrical supply)**

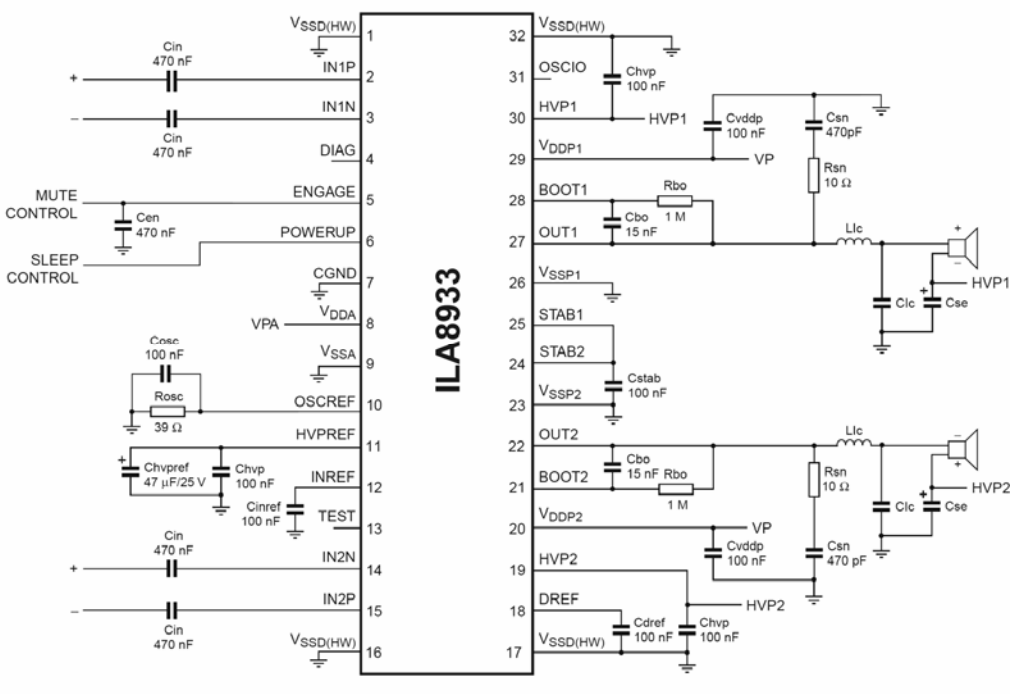



**Fig.5 Application diagram for 2 × SE (asymmetrical supply)**

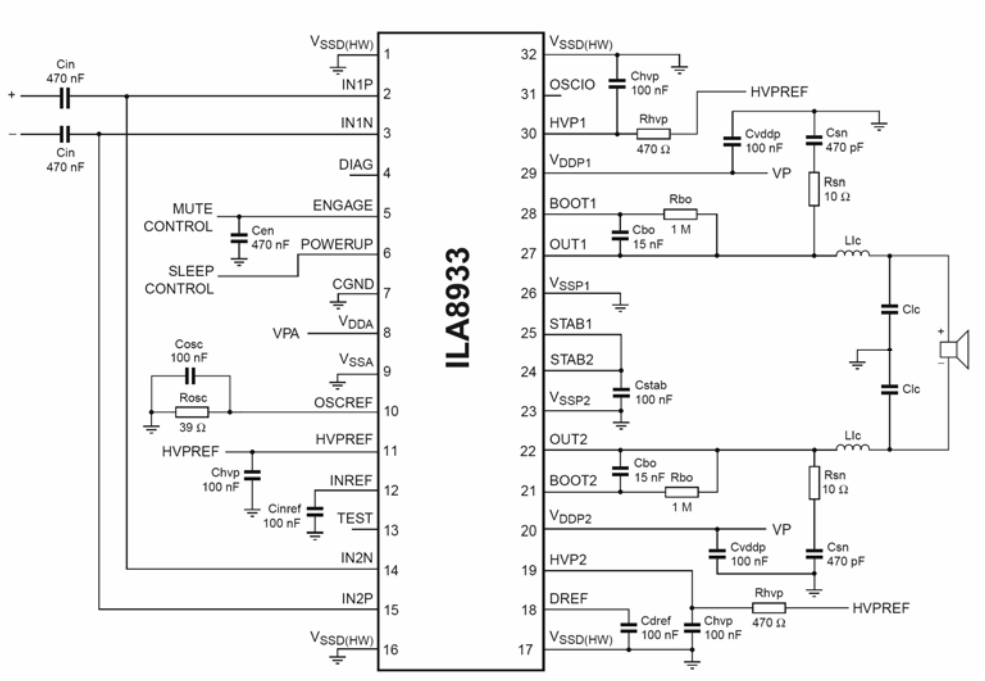
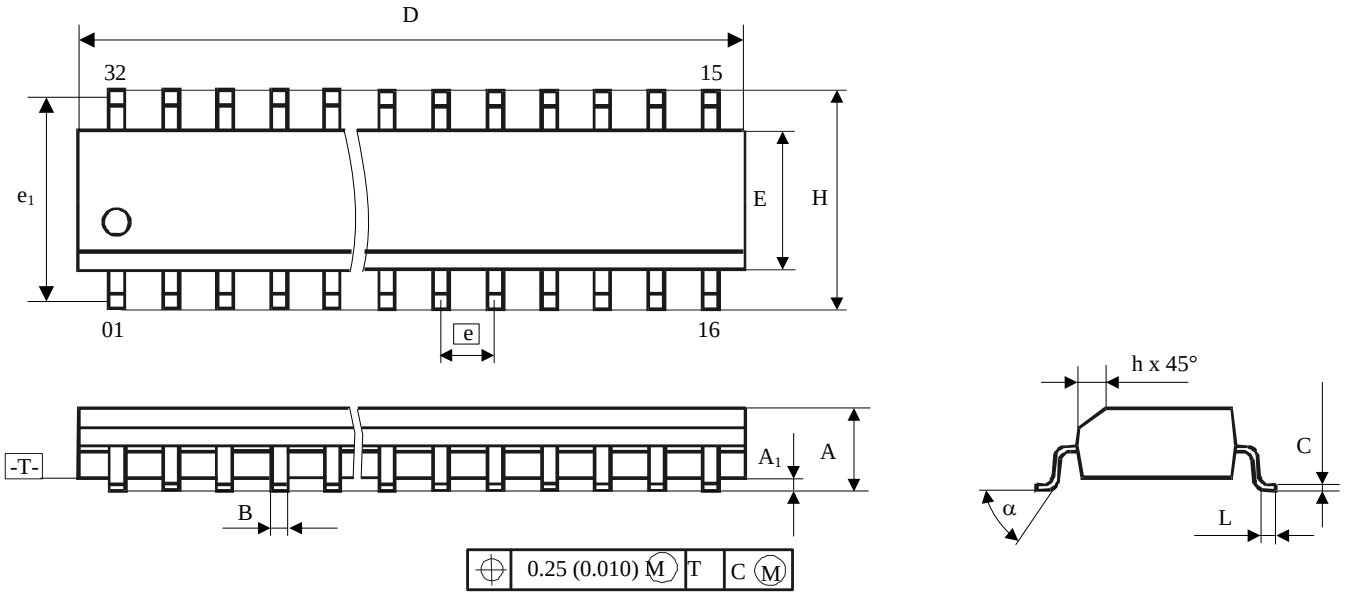



**Fig.6 Application diagram for 1 × BTL (asymmetrical supply)**




| | A | $A_1$ | B | C | D | E | e | H | h | L | α |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | mm | | | | | | | | | | degree |
| min | 2.65 | 0.1 | 0.35 | 0.14 | 20.3 | 7.4 | 1.27 (nom) | 10.0 | 0.25 | 0.40 | 0 |
| max | 3.05 | 0.3 | 0.50 | 0.32 | 20.7 | 7.6 | | 10.7 | 0.75 | 1.27 | 8 |

**Figure 5 – SO - package**