

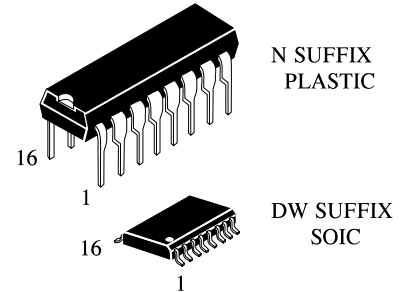
# IW4020B

## 14 STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDER

### High-Voltage Silicon-Gate CMOS

The IW4020B is ripple-carry binary counter. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):  
 1.0 V min @ 5.0 V supply  
 2.0 V min @ 10.0 V supply  
 2.5 V min @ 15.0 V supply



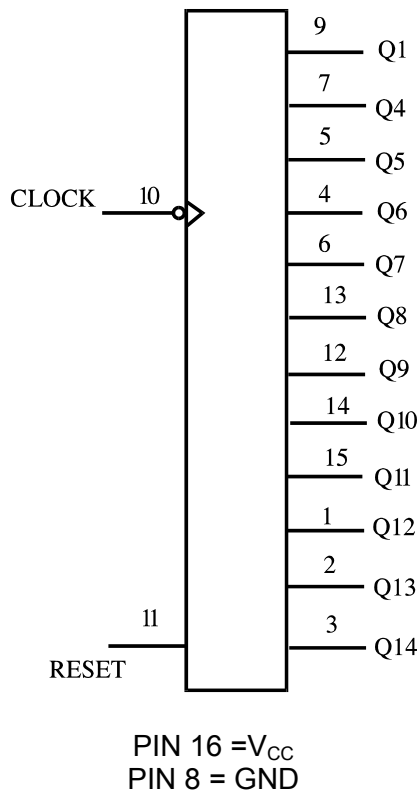
### ORDERING INFORMATION

IW4020BN Plastic

IW4020BDW SOIC

$T_A = -55^\circ$  to  $125^\circ$  C for all packages

### LOGIC DIAGRAM



### PIN ASSIGNMENT

Q12	1	16	$V_{CC}$
Q13	2	15	Q11
Q14	3	14	Q10
Q6	4	13	Q8
Q5	5	12	Q9
Q7	6	11	RESET
Q4	7	10	CLOCK
GND	8	9	Q1

### FUNCTION TABLE

Inputs		Output
Clock	Reset	Output state
	L	No change
	L	Advance to next state
X	H	All Outputs are low

X=don't care

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### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
$V_{IN}$	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$V_{OUT}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{IN}$	DC Input Current, per Pin	$\pm 10$	mA
$P_D$	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
$P_D$	Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	3.0	18	V
$V_{IN}, V_{OUT}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter		Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
					≥-55°C	25°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	High-Input	V <sub>OUT</sub> =0.5V or V <sub>CC</sub> - 0.5V	5.0	3.5	3.5	3.5	V
			V <sub>OUT</sub> =1.0V or V <sub>CC</sub> - 1.0V	10	7	7	7	
			V <sub>OUT</sub> =1.5V or V <sub>CC</sub> - 1.5V	15	11	11	11	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	Low-Input	V <sub>OUT</sub> =0.5V or V <sub>CC</sub> - 0.5V	5.0	1.5	1.5	1.5	V
			V <sub>OUT</sub> =1.0V or V <sub>CC</sub> - 1.0V	10	3	3	3	
			V <sub>OUT</sub> =1.5V or V <sub>CC</sub> - 1.5V	15	4	4	4	
V <sub>OH</sub>	Minimum High-Level Output Voltage	High-Output	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	4.95	4.95	4.95	V
				10	9.95	9.95	9.95	
				15	14.95	14.95	14.95	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	Low-Output	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	0.05	0.05	0.05	V
				10	0.05	0.05	0.05	
				15	0.05	0.05	0.05	
I <sub>IN</sub>	Maximum Input Leakage Current		V <sub>IN</sub> = GND or V <sub>CC</sub>	18	±0.1	±0.1	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)		V <sub>IN</sub> = GND or V <sub>CC</sub>	5.0 10 15 20	5 10 20 100	5 10 20 100	150 300 600 3000	μA
I <sub>OL</sub>	Minimum Low Output Current (Sink)	Output (Sink)	V <sub>IN</sub> = GND or V <sub>CC</sub>					mA
			U <sub>OL</sub> =0.4 V	5.0	0.64	0.51	0.36	
			U <sub>OL</sub> =0.5 V	10	1.6	1.3	0.9	
I <sub>OH</sub>	Minimum High Output Current (Source)	Output (Source)	V <sub>IN</sub> = GND or V <sub>CC</sub>					mA
			U <sub>OH</sub> =2.5 V	5.0	-2.0	-1.6	-1.15	
			U <sub>OH</sub> =4.6 V	5.0	-0.64	-0.51	-0.36	
			U <sub>OH</sub> =9.5 V	10	-1.6	-1.3	-0.9	
			U <sub>OH</sub> =13.5 V	15	-4.2	-3.4	-2.4	

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### AC ELECTRICAL CHARACTERISTICS ( $C_L=50\text{pF}$ , $R_L=200\text{k}\Omega$ , Input $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55$ $^{\circ}\text{C}$	$25^{\circ}\text{C}$	$\leq 125$ $^{\circ}\text{C}$	
$f_{\text{max}}$	Maximum Clock Frequency(Figure 1)	5.0	3.5	3.5	1.75	MHz
		10	8	8	4	
		15	12	12	6	
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Maximum Propagation Delay, Clock to Q1 (Figure 1)	5.0	360	360	720	ns
		10	160	160	320	
		15	130	130	260	
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Maximum Propagation Delay, $Q_n$ to $Q_{n+1}$ (Figure 3)	5.0	330	330	660	ns
		10	80	80	160	
		15	60	60	120	
$t_{\text{PHL}}$	Maximum Propagation Delay, Reset to Any Q (Figure 2)	5.0	280	280	560	ns
		10	120	120	240	
		15	100	100	200	
$t_{\text{TLH}}$ , $t_{\text{THL}}$	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
$C_{\text{IN}}$	Maximum Input Capacitance	-		7.5		pF

### TIMING REQUIREMENTS ( $C_L=50\text{pF}$ , $R_L=200\text{k}\Omega$ , Input $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55$ $^{\circ}\text{C}$	$25^{\circ}\text{C}$	$\leq 125^{\circ}$ C	
$t_w$	Minimum Pulse Width, Clock (Figure 1)	5.0	140	140	280	ns
		10	60	60	120	
		15	40	40	80	
$t_w$	Minimum Pulse Width, Reset (Figure 2)	5.0	200	200	400	ns
		10	80	80	160	
		15	60	60	120	
$t_{\text{rem}}$	Minimum Removal Time, Reset(Figure 2)	5.0	350	350	700	ns
		10	150	150	300	
		15	100	100	200	
$t_r$ , $t_f$	Maximum Input Rise and Fall Times, Clock (Figure 1)	5.0	Unlimited			$\mu\text{s}$
		10				
		15				

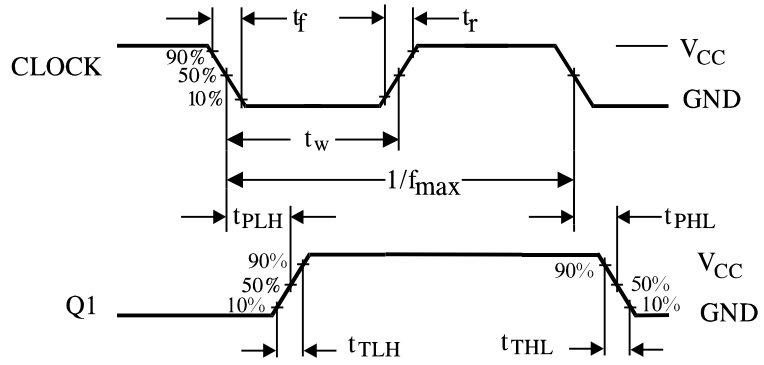


Figure 1. Switching Waveforms

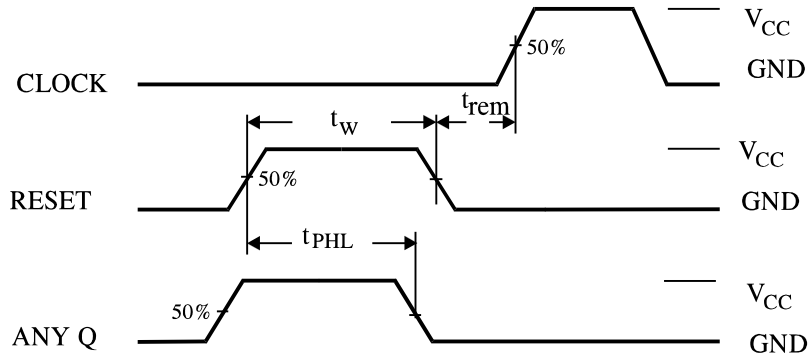


Figure 2. Switching Waveforms

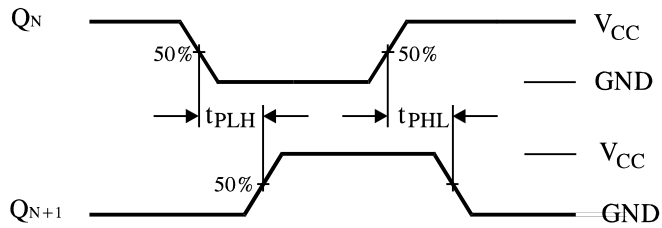
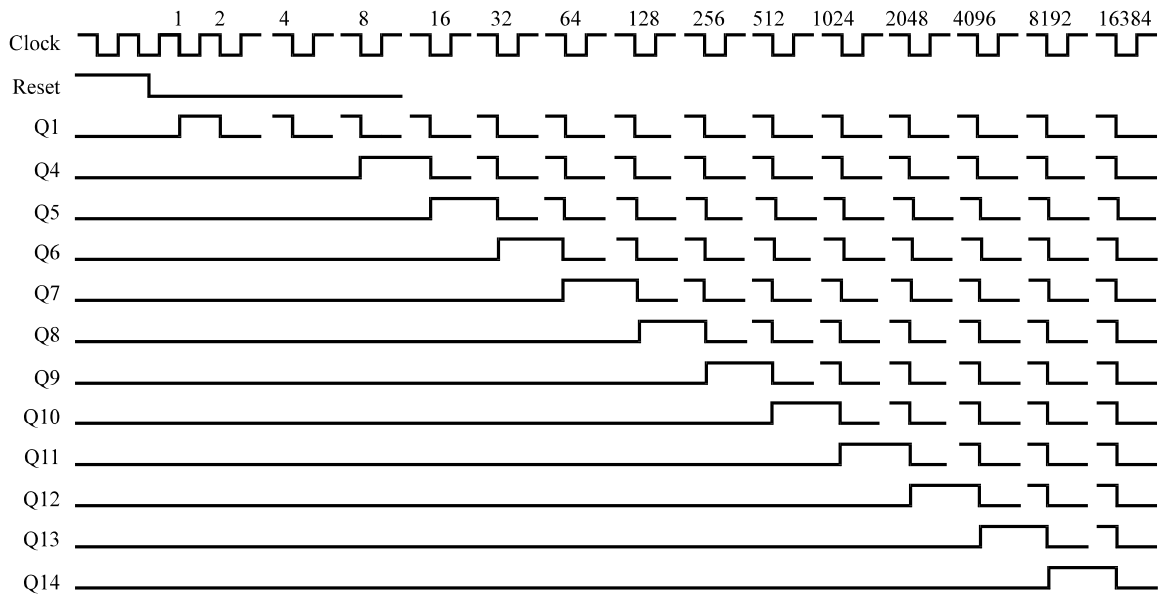


Figure 3. Switching Waveforms

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## TIMING DIAGRAM



## EXPANDED LOGIC DIAGRAM

