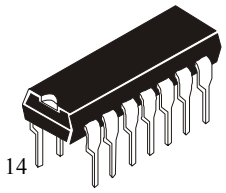
IL339N

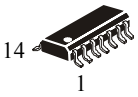
Quad Comparator

The IL339 consists of four independent voltage comparators with an offset voltage specification as low as 2.0 mV typ. The comparators operate in a wide range of voltages.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates.



N SUFFIX
PLASTIC



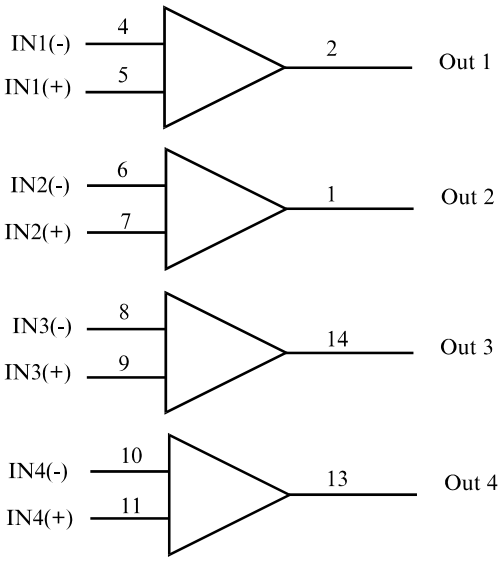
D SUFFIX
SOIC

- Single or Split Supply Operation
- Low Input Bias Current
- Low Input Offset Current
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage
- TTL and CMOS Compatible

ORDERING INFORMATION

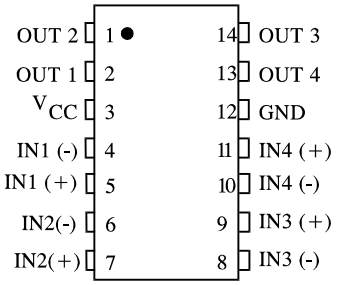
IL339N	Plastic
IL339D	SOIC
IZ339	Chip

BLOCK DIAGRAM



PIN 3 = V_{CC}
PIN 12 = GND

PIN ASSIGNMENT



INTEGRAL

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltages Single Supply Split Supplies	 36 ±18	 V
V_{IDR}	Input Differential Voltage Range	36	V
V_{ICR}	Input Common Mode Voltage Range (1)	-0.3 to V_{CC}	V
t_S	Short-Circuit duration of Output	100	ms
I_{IN}	Input Current, per pin (2)	50	mA
T_J	Junction Temperature Plastic Package	 150	 °C
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1mm from Case for 10 Seconds	260	°C
P_D	Power Dissipation T_A=+25°C Plastic Package Derate above 25°C	 1.0 8.0	 W mW/°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
Notes:
1. Split Power Supplies.
2. V_{IN}<-0.3V.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	±2.5 or 5.0	±15 or 30	V
T_A	Operating Temperature, All Package Types	0	+70	°C

DC ELECTRICAL CHARACTERISTICS (T_A=0 to +70°C)

Symbol	Parameter	Test Conditions	Guaranteed Limit		Unit
			Min	Max	
V_{IO}	Input Offset Voltage	V_0=1.4V V_{CC}=5.0-30V;R_S≤100Ω V_{ICR}=0V - (V_{CC}-1.5)V	-	9.0 5,0*	mV
I_{IB}	Input Bias Current	V_0=1.4V V_{CC}=5.0-30V V_{ICR}=0V - (V_{CC}-1.5)V	-	400 250*	nA
I_{IO}	Input Offset Current	V_0=1.4V V_{CC}=5.0-30V V_{ICR}=0V - (V_{CC}-1.5)V	-	±150 ±50*	nA
V_{ICR}	Input Common Mode Voltage Range	V_{CC}=5.0-30V	0	V_{CC}-2.0V V_{CC}-1.5V*	V
I_{CC}	Supply Current	R_L=∞,V_{CC}=5.0V R_L=∞,V_{CC}=30V	- -	2.0* 2.5*	mA
A_{VOL}	Voltage Gain	V_{CC}=15V, R_L=15KΩ	50*	-	V/mV
I_{sink}	Output Sink Current	V_I(-)=1.0V, V_I(+)=0V, V_0≤1.5V, V_{CC}=5.0V	6.0*	-	mA
V_{sat}	Saturation Voltage	V_I(-)=1.0V, V_I(+)=0V, I_{sink}≤4.0mA, V_{CC}=5.0V	-	700 400*	mV
I_{OL}	Output Leakage Current	V_I(+)=1.0V, V_I(-)=0V, V_0=5.0V V_0=30V		 1000	nA
V_{IDR}	Differential Input Voltage Range	All V_{IN}≥0		V_{CC}*	V

* T_A=+25°C

NOTE: Guaranteed Limits of DC Electrical Characteristics are given for T_A=0, + 70°C as the information for chips.

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{CC}=1.5V, T_A=+25°C (each comparator))

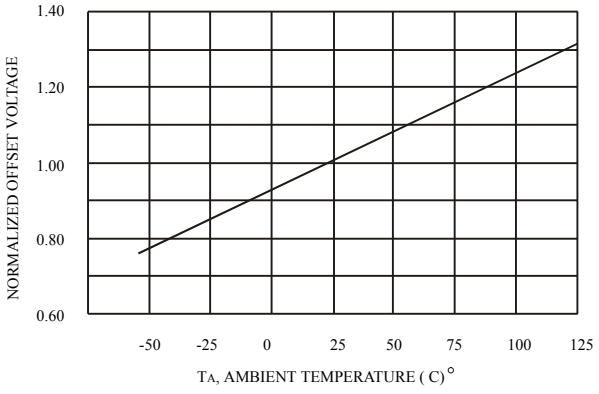


Figure 1. Normalized Input Offset Voltage

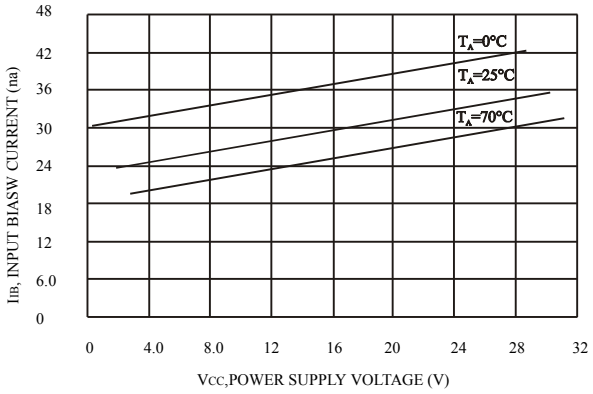


Figure 2. Input Bias Current

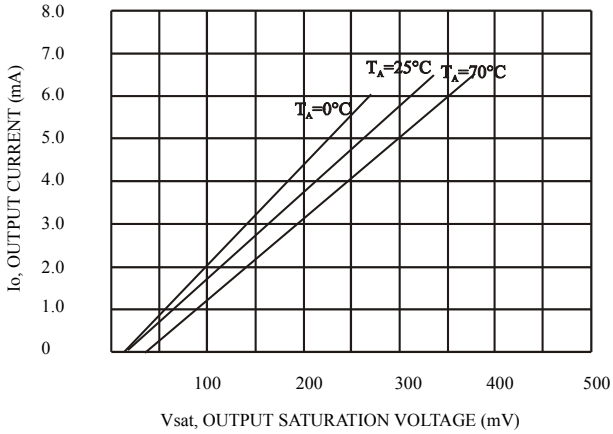
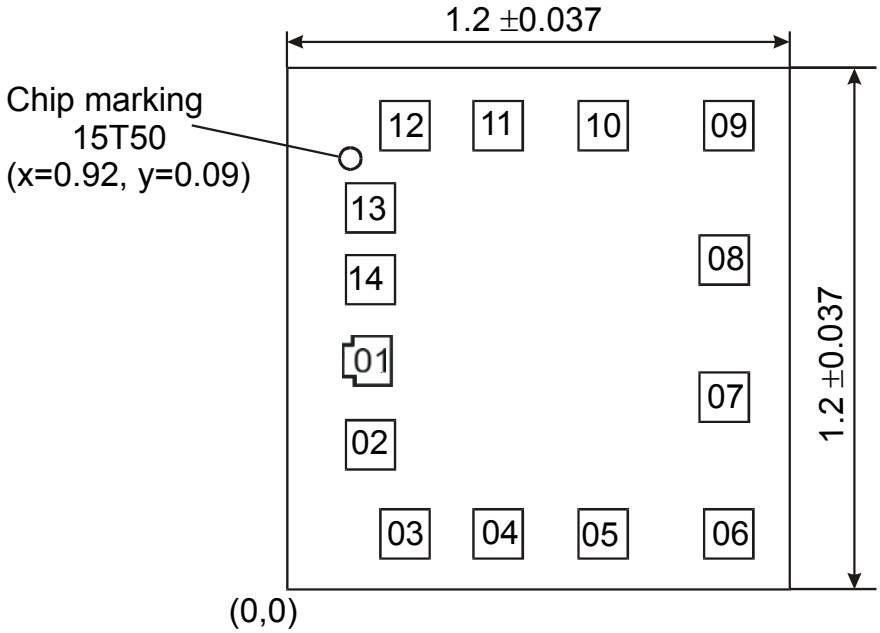


Figure 3. Output Sink Current versus Output Saturation Voltage

TYPICAL DC ELECTRICAL CHARACTERISTICS (T_A=+25°C)

Symbol	Parameter	Test Conditions	Value	Unit
t_1	Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{ref}=1.4V, V_{CC}=5.0V, R_L=5.1KΩ, V_{RL}=5.0V	300	ns
t_2	Response Time	V_{CC}=5.0V, R_L=5.1KΩ, V_{RL}=5.0V	1.3	µs

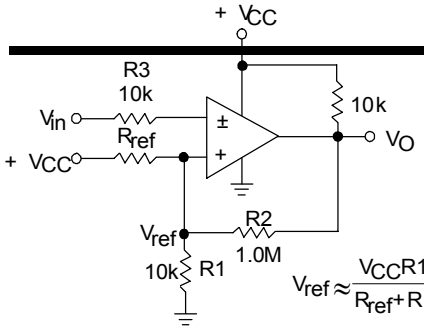
CHIP PAD DIAGRAM IZ339



Pad size 0.110 x 0.110 mm (Pad size is given as per passivation layer)
Thickness of chip 0,46±0,02 mm

PAD LOCATION

PAD NO	Symbol	X	Y
01	OUT2	0.100	0.462
02	OUT1	0.100	0.297
03	V_{CC}	0.180	0.100
04	IN1 (-)	0.385	0.100
05	IN1 (+)	0.672	0.100
06	IN2 (-)	0.990	0.100
07	IN2 (+)	0.990	0.377
08	IN3 (-)	0.990	0.712
09	IN3 (+)	0.990	0.990
10	IN4 (-)	0.672	0.990
11	IN4 (+)	0.385	0.990
12	GND	0.180	0.990
13	OUT4	0.100	0.793
14	OUT3	0.100	0.625



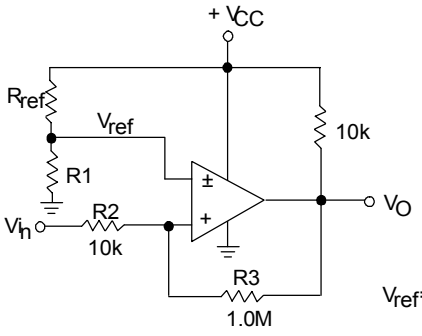
$$V_{ref} \approx \frac{V_{CC} R1}{R_{ref} + R1}$$

$$R3 \approx R1 // R_{ref} // R2$$

$$V_H = \frac{R1 // R_{ref}}{R1 // R_{ref} + R2} [V_{O(max)} - V_{O(min)}]$$

$$R2 > R_{ref} // R1$$

Figure 4. Inverting Comparator with Hystersis



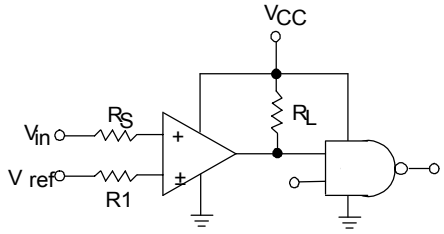
$$V_{ref} = \frac{V_{CC} R1}{R_{ref} + R1}$$

$$R2 \approx R1 // R_{ref}$$

Amount of Hysteresis V_H

$$V_H = \frac{R2}{R2 + R3} [(V_{O(max)} - V_{O(min)}]$$

Figure 5. Noninverting Comparator with Hysteresis

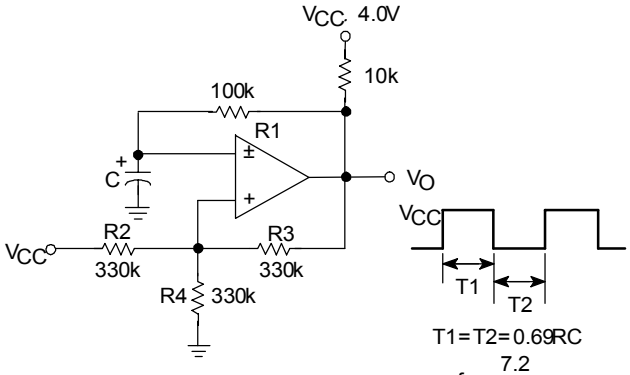


R_S = Source Resistance

$R1 \approx R_S$

Logic	Device	V_{CC} (V)	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

Figure 6. Driving Logic



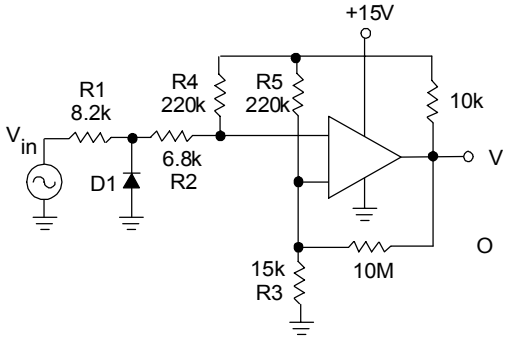
$$T1 = T2 = 0.69RC$$

$$f = \frac{7.2}{C(\mu F)}$$

$$R2 = R3 = R4$$

$$R1 \approx R2 // R3 // R4$$

Figure 7. Squarewave Oscillator



D1 prevents input from going negative by more than 0.6 V

$$R1 + R2 = R3$$

$$R3 \approx \frac{R5}{10} \text{ for small error in zero crossing}$$

Figure 8. Zero Crossing Detector (Single Supply)

$V_{in(min)} \approx 0.4V$ Peak for 1% phase distortion ($\Delta\Theta$).

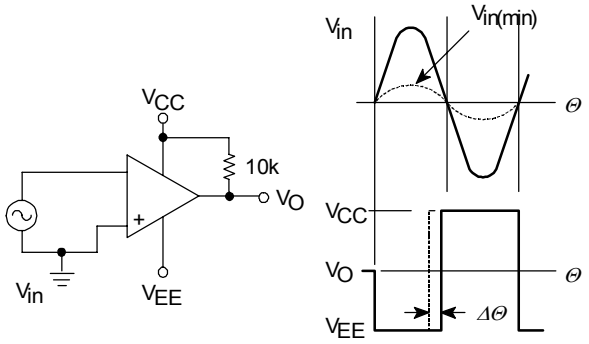


Figure 9. Zero Crossing Detector (Split Supplies)

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