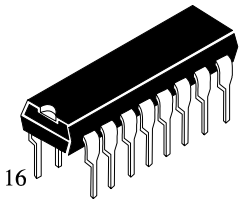
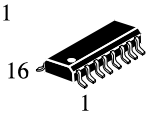
IN74AC139

Dual 1-of-4 Decoder/Demultiplexer



N SUFFIX
PLASTIC



D SUFFIX
SOIC

ORDERING INFORMATION

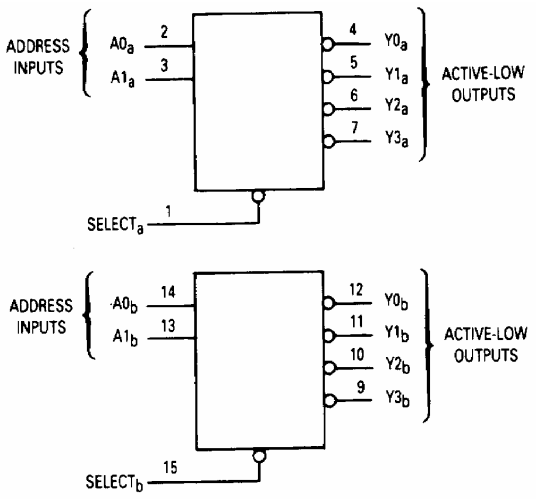
IN74AC139N Plastic
IN74AC139D SOIC
IZ74AC139 Chip
T_A = -45° to 85° C for all packages

The IN74AC139 is identical in pinout to the LS/ALS139, HC/HCT139. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALS outputs.

This device consists of two independent 1-of-4 decoders, each of which decodes a two-bit Address to one-of-four active-low outputs. Active-low Selects are provided to facilitate the demultiplexing and cascading functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and utilizing the Select as a data input.

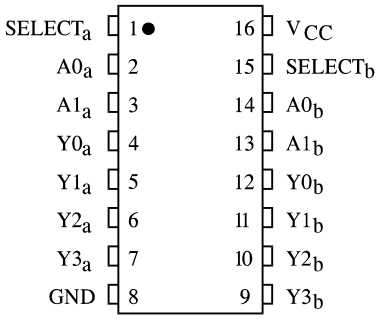
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA; 0.1 μA @ 25°C
- High Noise Immunity Characteristic of CMOS Devices
- Outputs Source/Sink 24 mA

LOGIC DIAGRAM



PIN 16 =V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs			
Select	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X = don’t care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
**Derating - Plastic DIP: - 10 mW/°C from 65° to 85°C
SOIC Package: : - 7 mW/°C from 65° to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Temperature, All Package Types		-45	+85	°C
I_{OH}	Output Current - High			-24	mA
I_{OL}	Output Current - Low			24	mA
t_r, t_f	Input Rise and Fall Time * (except Schmitt Inputs)	V_{CC} =3.0 V V_{CC} =4.5 V V_{CC} =5.5 V	0 0 0	150 40 25	ns/V

* V_{IN} from 30% to 70% V_{CC}

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limits		Unit
				25 °C	-45°C to 85°C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V	3.0 4.5 5.5	2.1 3.15 3.85	2.1 3.15 3.85	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V	3.0 4.5 5.5	0.9 1.35 1.65	0.9 1.35 1.65	V
V_{OH}	Minimum High-Level Output Voltage	$I_{OUT} \leq$ -50 μA	3.0 4.5 5.5	2.9 4.4 5.4	2.9 4.4 5.4	V
		*V_{IN}=V_{IH} or V_{IL} I_{OH}=-12 mA I_{OH}=-24 mA I_{OH}=-24 mA	 3.0 4.5 5.5	 2.56 3.86 4.86	 2.46 3.76 4.76	
V_{OL}	Maximum Low-Level Output Voltage	$I_{OUT} \leq$ 50 μA	3.0 4.5 5.5	0.1 0.1 0.1	0.1 0.1 0.1	V
		*V_{IN}=V_{IH} or V_{IL} I_{OL}=12 mA I_{OL}=24 mA I_{OL}=24 mA	 3.0 4.5 5.5	 0.36 0.36 0.36	 0.44 0.44 0.44	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	5.5	±0.1	±1.0	μA
I_{OLD}	**Minimum Dynamic Output Current	V_{OLD}=1.65 V Max	5.5		75	mA
I_{OHD}	**Minimum Dynamic Output Current	V_{OHD}=3.85 V Min	5.5		-75	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND	5.5	8.0	80	μA

* All outputs loaded; thresholds on input associated with output under test.

**Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}

AC ELECTRICAL CHARACTERISTICS (C_L=50pF,Input t_r=t_f=3.0 ns)

Symbol	Parameter	V_{CC}* V	Guaranteed Limits				Unit
			25 °C		-45°C to 85°C		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay , Input A to Output Y (Figure 2)	3.3 5.0	4.0 3.0	11.5 8.5	3.5 2.5	13 9.5	ns
t_{PHL}	Propagation Delay , Input A to Output Y (Figure 2)	3.3 5.0	3.0 2.5	10 7.5	2.5 2.0	11 8.5	ns
t_{PLH}	Propagation Delay, Select to Output Y (Figure 1)	3.3 5.0	4.5 3.5	12 8.5	3.5 3.0	13 10	ns
t_{PHL}	Propagation Delay, Select to Output Y (Figure 1)	3.3 5.0	4.0 2.5	10 7.5	3.0 2.5	11 8.5	ns
C_{IN}	Maximum Input Capacitance	5.0	4.5		-		pF

		Typical @25°C,V_{CC}=5.0 V	
C_{PD}	Power Dissipation Capacitance	40	pF

*Voltage Range 3.3 V is 3.3 V ±0.3 V
Voltage Range 5.0 V is 5.0 V ±0.5 V

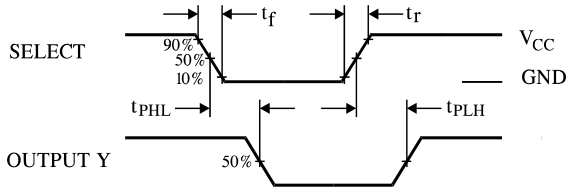


Figure 1. Switching Waveform

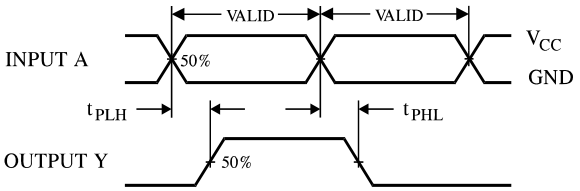
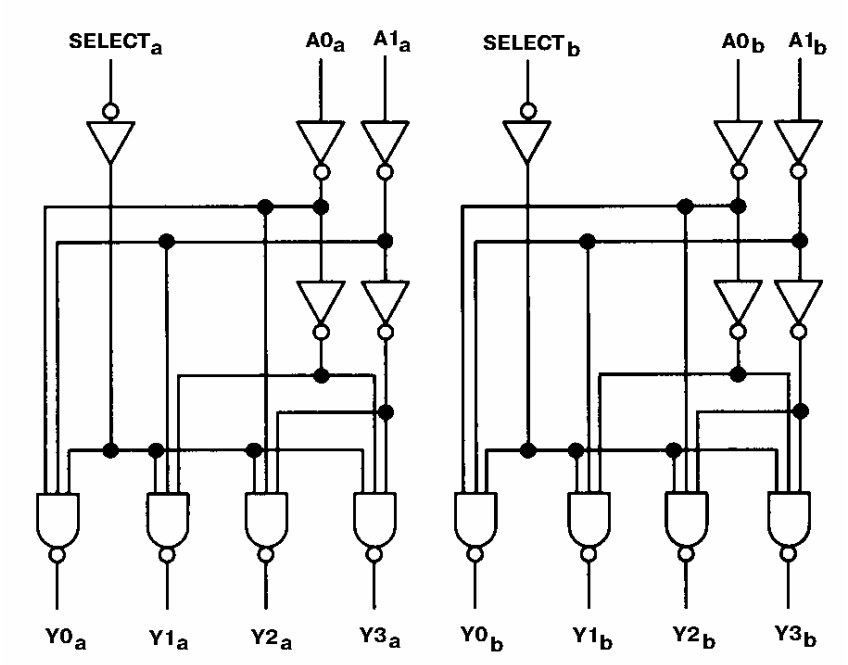
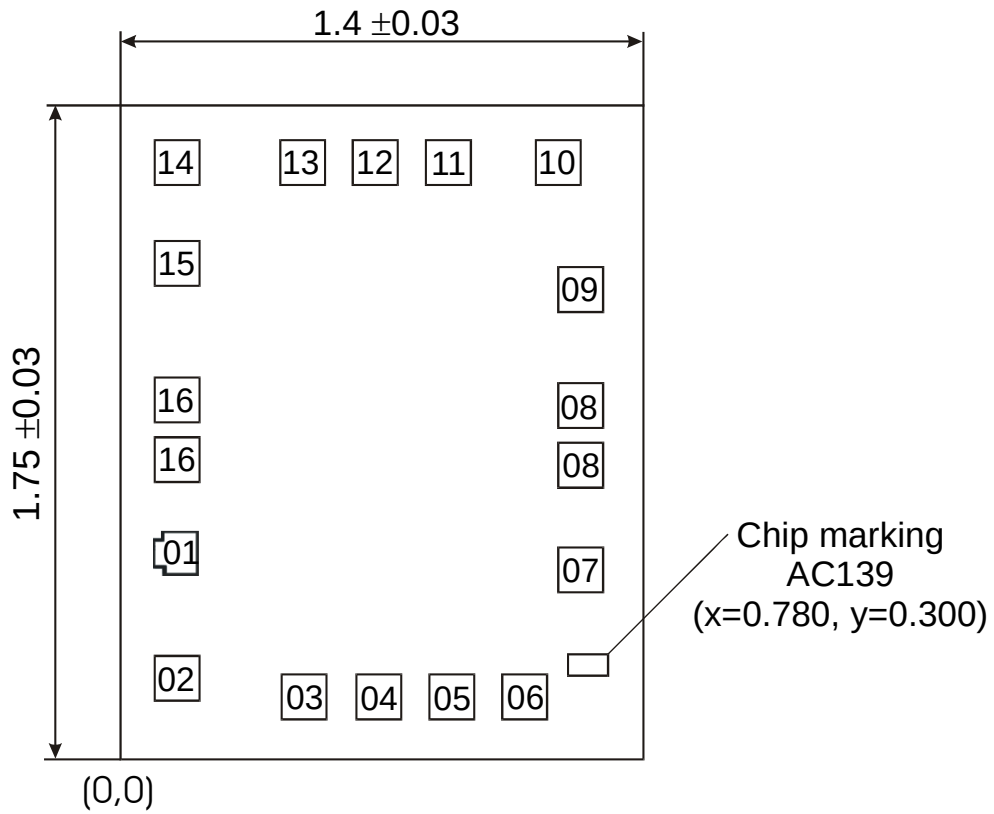


Figure 2. Switching Waveform

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM IZ74AC139



Thickness of chip 0,46±0,02 mm
Pad size 0.120x0.120 mm (Pad size is given as per metallization layer

PAD LOCATION

Pad No	Symbol	X	Y
01	SELECT a	0.100	0.487
02	A0a	0.100	0.150
03	A1a	0.440	0.100
04	Y0a	0.640	0.100
05	Y1a	0.835	0.100
06	Y2a	1.030	0.100
07	Y3a	1.180	0.440
08	GND	1.180/1.180	0.720/0.880
09	Y3b	1.180	1.190
10	Y2b	1.120	1.530
11	Y1b	0.826	1.530
12	Y0b	0.630	1.530
13	A1b	0.436	1.530
14	A0b	0.100	1.530
15	SELECT b	0.100	1.260
16	Vcc	0.100/0.100	0.895/0.735