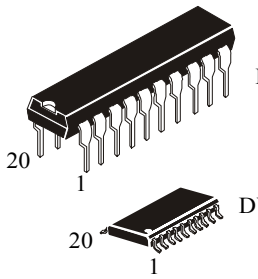
IN74HC573A

Octal 3-State Noninverting Transparent Latch

High-Performance Silicon-Gate CMOS



N SUFFIX
PLASTIC DIP

DW SUFFIX
SOIC

ORDERING INFORMATION

IN74HC573AN	Plastic DIP
IN74HC573ADW	SOIC
IZ74HC573A	chip

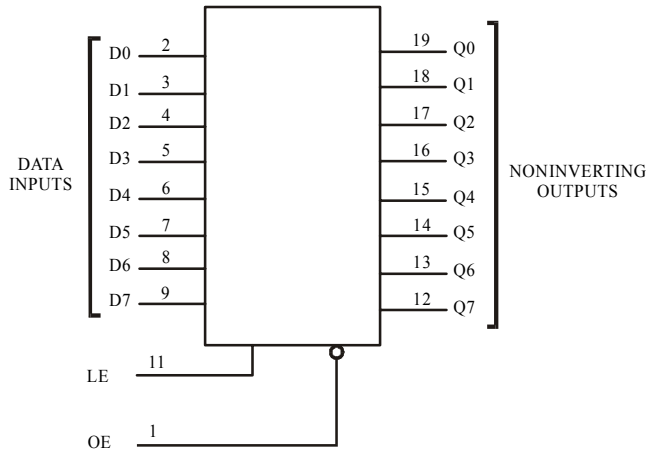
T_A = -55° to 125° C for all packages

The IN74HC573A is identical in pinout to the LS/ALS573. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

These latches appear transparent to data (i.e., the outputs change asynchronously) when LE is high. When LE goes low, data meeting the setup and hold time becomes latched.

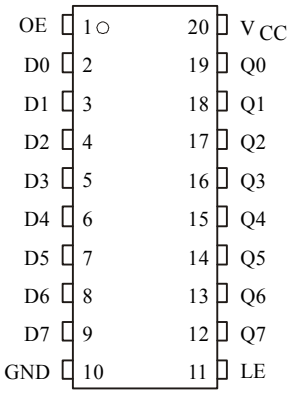
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices

LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
OE	**LE**	**D**	**Q**
L	H	H	H
L	H	L	L
L	L	X	no change
H	X	X	Z

H= high level
L = low level
X = don't care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm from Case for 4 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	$V_{OUT} \geq V_{CC}$-0.1 V $\lvert I_{OUT} \rvert \leq 20$ μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low -Level Input Voltage	$\lvert V_{OUT} \rvert \leq 0.1$ V $\lvert I_{OUT} \rvert \leq 20$ μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN}=V_{IH}$ $\lvert I_{OUT} \rvert \leq 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{IN}=V_{IH}$ $\lvert I_{OUT} \rvert \leq 6.0$ mA $\lvert I_{OUT} \rvert \leq 7.8$ mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN}= V_{IL}$ $\lvert I_{OUT} \rvert \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{IN}= V_{IL}$ $\lvert I_{OUT} \rvert \leq 6.0$ mA $\lvert I_{OUT} \rvert \leq 7.8$ mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	$V_{IN}=V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three State Leakage Current	Output in High-Impedance State $V_{IN} = V_{IH}$ $V_{OUT}= V_{CC}$ or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0$μA	6.0	4.0	40	160	μA

AC ELECTRICAL CHARACTERISTICS(C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input D to Q (Figures 1 and 5)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, LE to Q (Figures 2 and 5)	2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, OE to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{PZH}, t_{PZL}	Maximum Propagation Delay, OE to Q (Figures 3 and 6)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 5)	2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF
C_{OUT}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	-	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 23	pF

TIMING REQUIREMENTS (C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{SU}	Minimum Setup Time, Input D to Latch Enable (Figure 4)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_h	Minimum Hold Time, Latch Enable to Input D (Figure 4)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_w	Minimum Pulse Width, Latch Enable (Figure 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

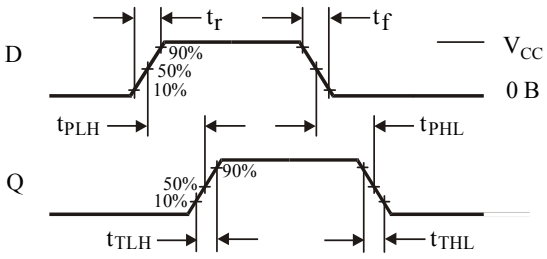


Figure 1. Switching Waveforms

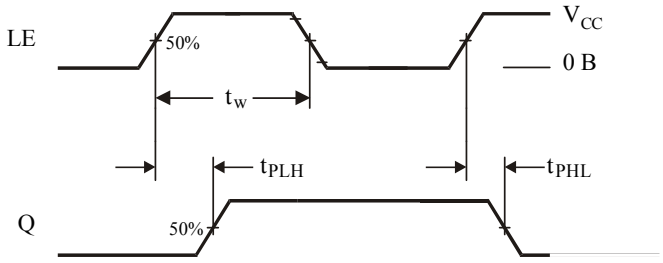


Figure 2. Switching Waveforms

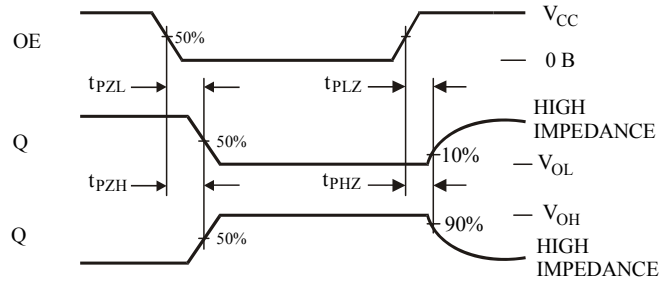


Figure 3. Switching Waveforms

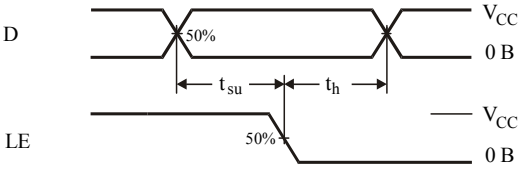
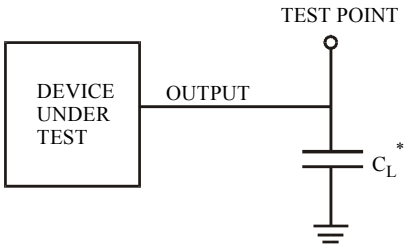
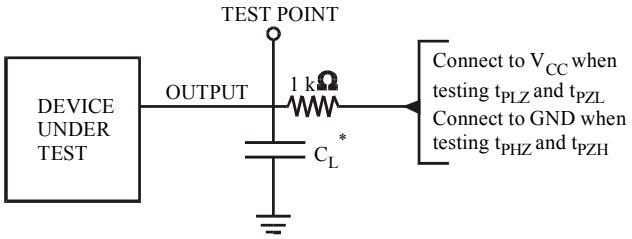


Figure 4. Switching Waveforms



* Includes all probe and jig capacitance

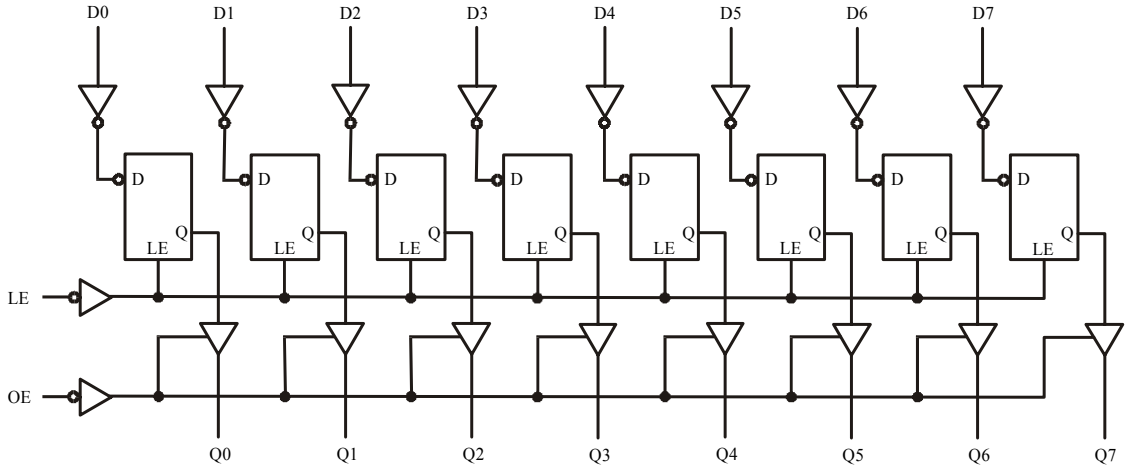
Figure 5. Test Circuit



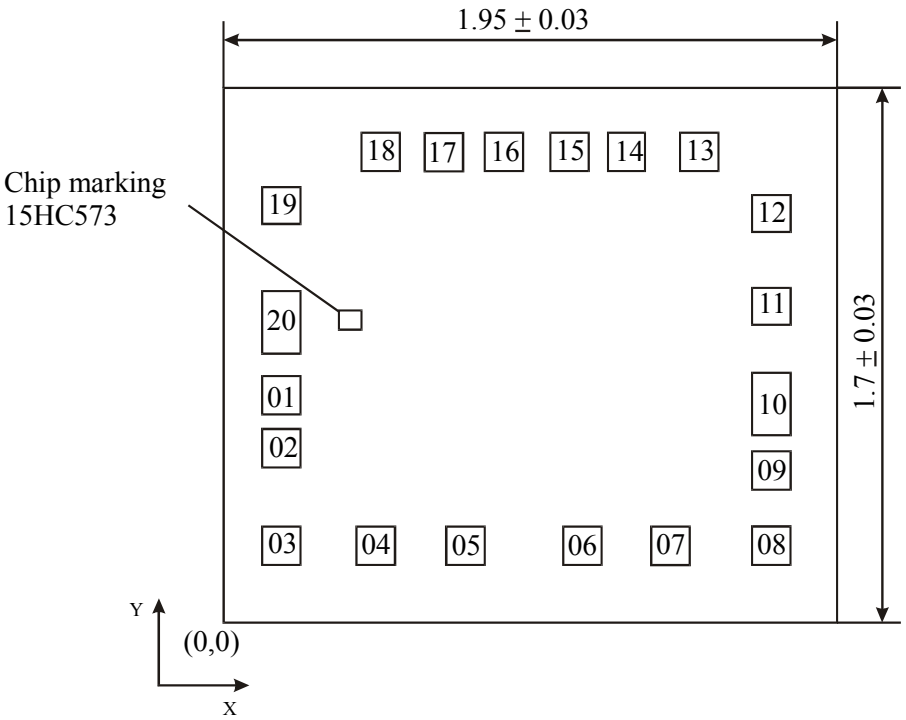
* Includes all probe and jig capacitance

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x=0.370, y=0.929; right higher corner x=0.443, y=0.995.

Chip thickness: 0.46 ± 0.02 mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	OE	0.126	0.665	0.12 x 0.12
02	D0	0.126	0.495	0.12 x 0.12
03	D1	0.126	0.185	0.12 x 0.12
04	D2	0.425	0.185	0.12 x 0.12
05	D3	0.71	0.185	0.12 x 0.12
06	D4	1.08	0.185	0.12 x 0.12
07	D5	1.36	0.185	0.12 x 0.12
08	D6	1.68	0.185	0.12 x 0.12
09	D7	1.68	0.425	0.12 x 0.12
10	GND	1.68	0.595	0.12 x 0.2
11	LE	1.68	0.945	0.12 x 0.12
12	Q7	1.68	1.24	0.12 x 0.12
13	Q6	1.45	1.435	0.12 x 0.12
14	Q5	1.22	1.435	0.12 x 0.12
15	Q4	1.04	1.435	0.12 x 0.12
16	Q3	0.83	1.435	0.12 x 0.12
17	Q2	0.64	1.435	0.12 x 0.12
18	Q1	0.44	1.435	0.12 x 0.12
19	Q0	0.126	1.265	0.12 x 0.12
20	V_{CC}	0.126	0.855	0.12 x 0.2

Note: Pad location is given as per metallization layer