Intelligent 104-Bit EEPROM Counter for > 20000 Units with Security Logic

The chip contains an EEPROM/PROM of 88 bits, a mask ROM of 16 bits and a sequencing control with security logic.
Memory (104 bits) is divided into the following functional areas
In the condition as supplied, the transport code and the error counter are activated. The chip can only be read (except for the transport-code area) and only the error counter can be written.
Following correct entry of the transport code, the entire memory can be read and areas II and III can be written and EEPROM part of area III can be erased.
After the control flag has been written, everything is readable and only area III can be programmed, but with the following changes:
- The transport code and the error counter are no longer activated.
- The area of the former transport code and the error counter can be erased byte by byte with carry.
- The entire area III can be written bit by bit

NB: When the control flag is written, the counter stage below it (the error counter) can be erased at the same time.

FEATURES

- 104 x 1 bit organization
- Three memory areas with special characteristics (eg ROM, PROM, EEPROM)
- Maximum of 20480 count units
- Special security features
- Minimum of 10^4 write/erase cycles
- Data retention for minimum of ten years
- Contact configuration and serial interface in accordance to ISO standard 7816-3 (synchronous transmission)

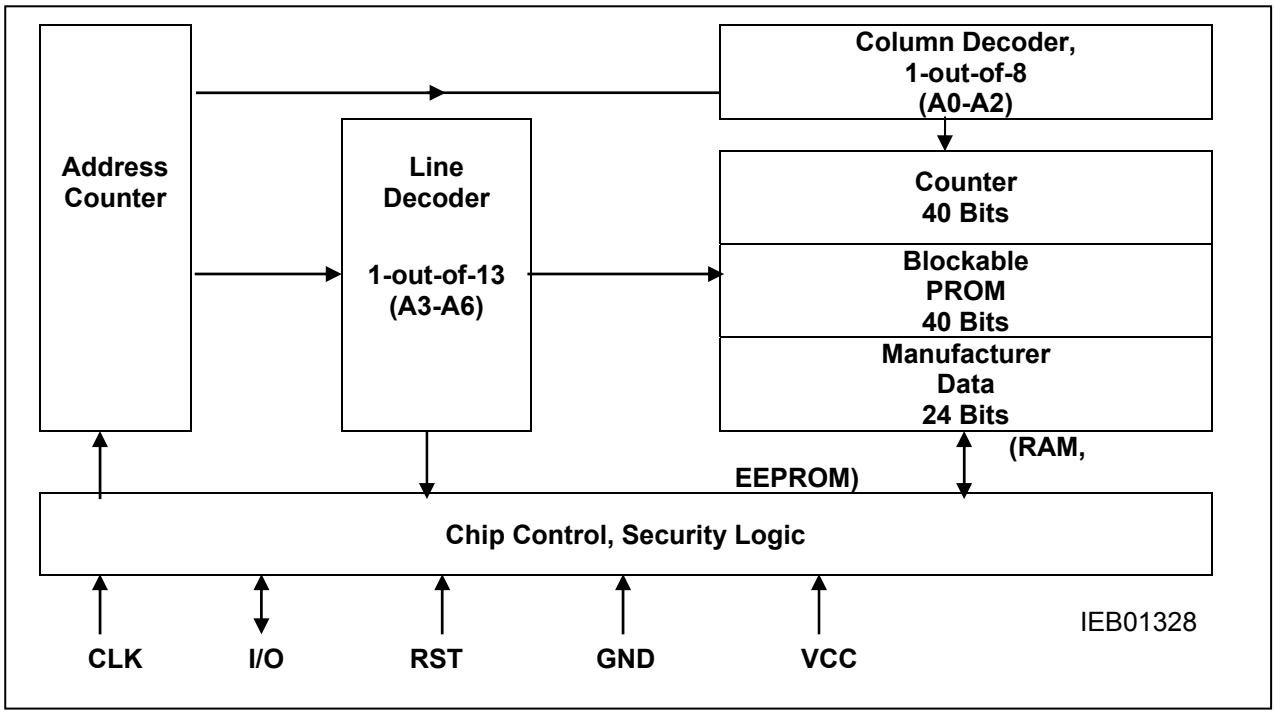
PIN DEFINITIONS AND FUNCTIONS

Card Contact	Pad №	Symbol	Function
C7	01	I/O	Bidirectional data line (open drain) Code entry on “Input” only for transport
	02	P	Test input
C3	03	CLC	Clock input
C2	04	RST	Control input (reset)
C1	05	Vcc	Supply voltage
C6		N.C.	Not connected
C5	06	GND	Ground

IZ4406 comes as an M1 wire-bonded module for embedding in plastic cards and as a die for customer packaging

I	ROM	This area contains unalterable chip data (eg application, design status). Part of the data is entered by way of a ROM mask and the remainder when testing. Both parts are unalterable.
II	PROM	In this area the user can enter card data for a particular application. A control flag can be set to safeguard this area against alteration.
III	PROM/EEPROM	This area contains the count data and stores the current count in nonvolatile memory. The individual counter stages with carry can be erased (ie EEPROM), only the uppermost counter stage not being erasable (ie PROM). Before the control flag is set, part of the EEPROM area contains a secret transport code. Another part serves as an error counter. Function of the PROM area: 1 bit: Control flag 3 bits: Test bits for manufacturer 4 bits: for user

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit Values		Unit	Comments
		Min.	Max.		
Supply voltage	V_{CC}	-0.3	6	V	-
Input voltage	V_I	-0.3	6	V	-
Storage temperature	T_{stg}	-60	125	°C	
Power dissipation	P_{tot}		27,5	MW	-

OPERATING RANGE

Parameter	Symbol	Limit Values		Unit	Comments
		Min.	Max.		
Supply voltage	V_{CC}	4.75	5.5	V	-
Ambient temperature	T_A	-35	80	°C	-

DC CHARACTERISTICS

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
SUPPLY						
Supply voltage	V_{CC}	4.75	5	5.5	V	-
Supply current	I_{CC}		1.5	5	mA	-
DATA INPUT						
H-Input voltage (I/O,CLC,P,RST)	V_H	3.5	-	V_{CC}	V	-
L-Input voltage (I/O,CLC,RST)	V_L	0	-	0.8	V	-
L-Input current (CLC) (V_H=5 V, internal pull-down)	I_H	-	-	100	µA	-
L-Input current (RST) (V_H=0 V, internal pull-up)	$-I_L$	-	-	100	µA	-
DATA OUTPUT						
L-Output current (V_H=0.5 V, open drain)	I_L	-	-	0.5	µA	-
H-Output current (V_H=5 V, open drain)	I_H	-	-	10	µA	-

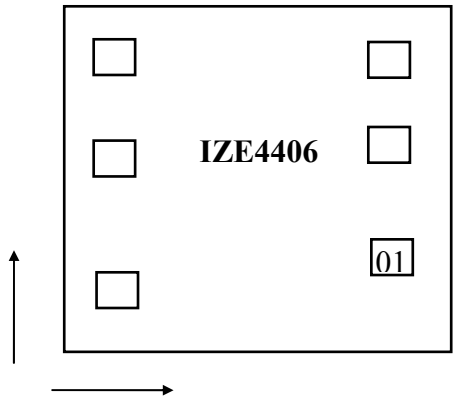
PULSE DURATION

RST (address reset)	t_R	50	-	-	µs	-
RST (set R – flag)	t_S	10	-	-	µs	-
CLC (count, H-level)	t_H	10	-	-	µs	-
CLC (count, L-level)	t_L	10	-	-	µs	-
CLC (write, H-level)	t_{HW}	5	-	-	ms	-
CLC (erase, H-level)	t_{HE}	5	-	-	ms	-

AC CHARACTERISTICS

Delay time	t_{d1}	5	-	-	µs	-
Delay time	t_{d2}	3.5	-	-	µs	-
Delay time	t_{d9}	5	-	-	µs	-
Delay time	t_{d10}	5	-	-	µs	-
Delay time	t_{d3}, t_{d4}, t_{d5}	3.5	-	-	µs	-
Delay time	t_{d6}, t_{d7}	5	-	-	µs	-
Delay time	t_{d8}	10	-	-	µs	-

CHIP PAD DIAGRAM



INTEGRAL

Chip Size (mm): x = 1,1±0.03 , y = 1,1± 0.03
Thickness of chip (mm): 0,18 ± 0,01

PAD DESCRIPTION

Pad No.	Symbol	Description
01	I/O	Bidirectional data line (open drain) Code entry on "Input" only for transport
02	P	Test input
03	CLC	Clock input
04	RST	Control input (reset)
05	Vcc	Supply voltage
06	GND	Ground

PAD LOCATION

Pad No.	Location (Left Lower corner), mm		Pad size, mm
	X	Y	
01	0.8530	0.2530	0,100 x 0,100
02	0.8530	0.6105	0,100 x 0,100
03	0.8530	0.8395	0,100 x 0,100
04	0.1530	0.8435	0,100 x 0,100
05	0.1530	0.5635	0,100 x 0,100
06	0,1440	0,1640	0,100 x 0,100